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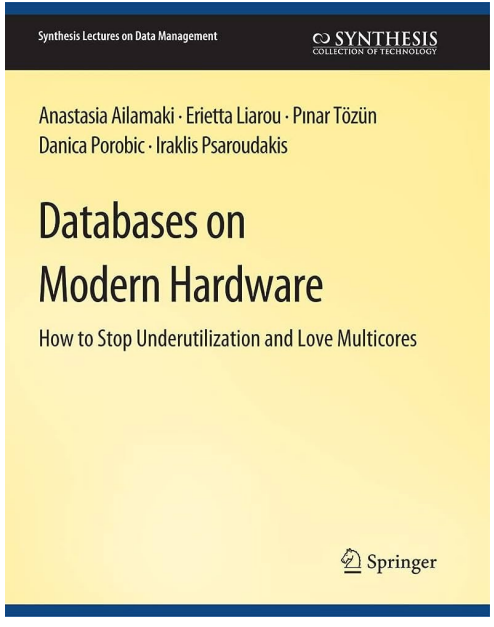
hardware parallelism & transaction processing systems

Pınar Tözün
Associate Professor,
IT University of Copenhagen
pito@itu.dk, www.pinartozun.com, @pinartozun



HPI – Lecture Series on DB Research
October 24, 2023

transaction vs. analytical processing

OLTP	OLAP
short-running simple requests	long-running complex requests
access small portion of the data	access lots of data
fetch several columns of a record	fetch a few columns of a record
lookup, insert, delete, update	SQL queries, map-reduce jobs, machine learning, graph analytics, …
deposit money to a customer's account, lookup information about a product, looking up a tweet, …	*customers who are most likely to get mortgages next year, item sold the most last year in each department of a store grouped by months, …*

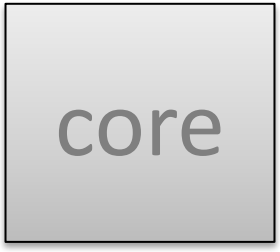
➔ **primary applications for databases**

➔ **required functionality & optimizations differ**

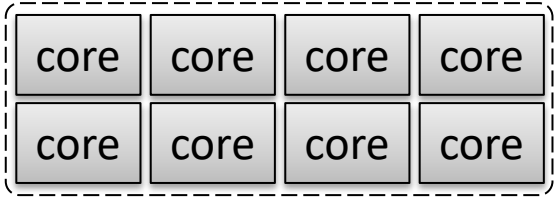
evolution of general-purpose CPU

… the hardware we run transactions on

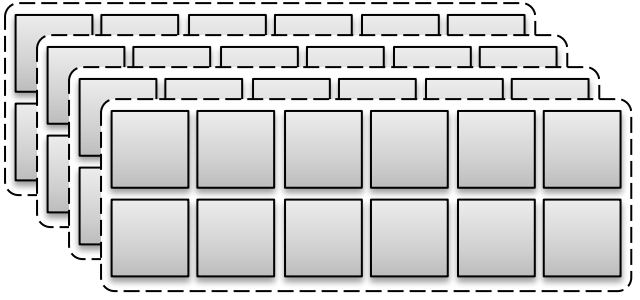
2005



single-core CPUs



multicore CPUs



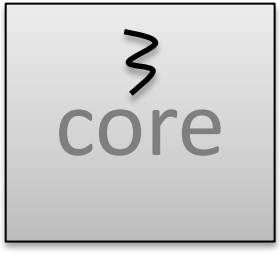
multisocket multicore CPUs

faster & more-complex cores over time

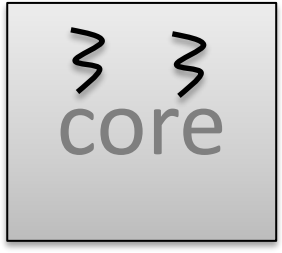
similar speed & complexity in a core, more cores over time

types of hardware parallelism

implicit/vertical parallelism



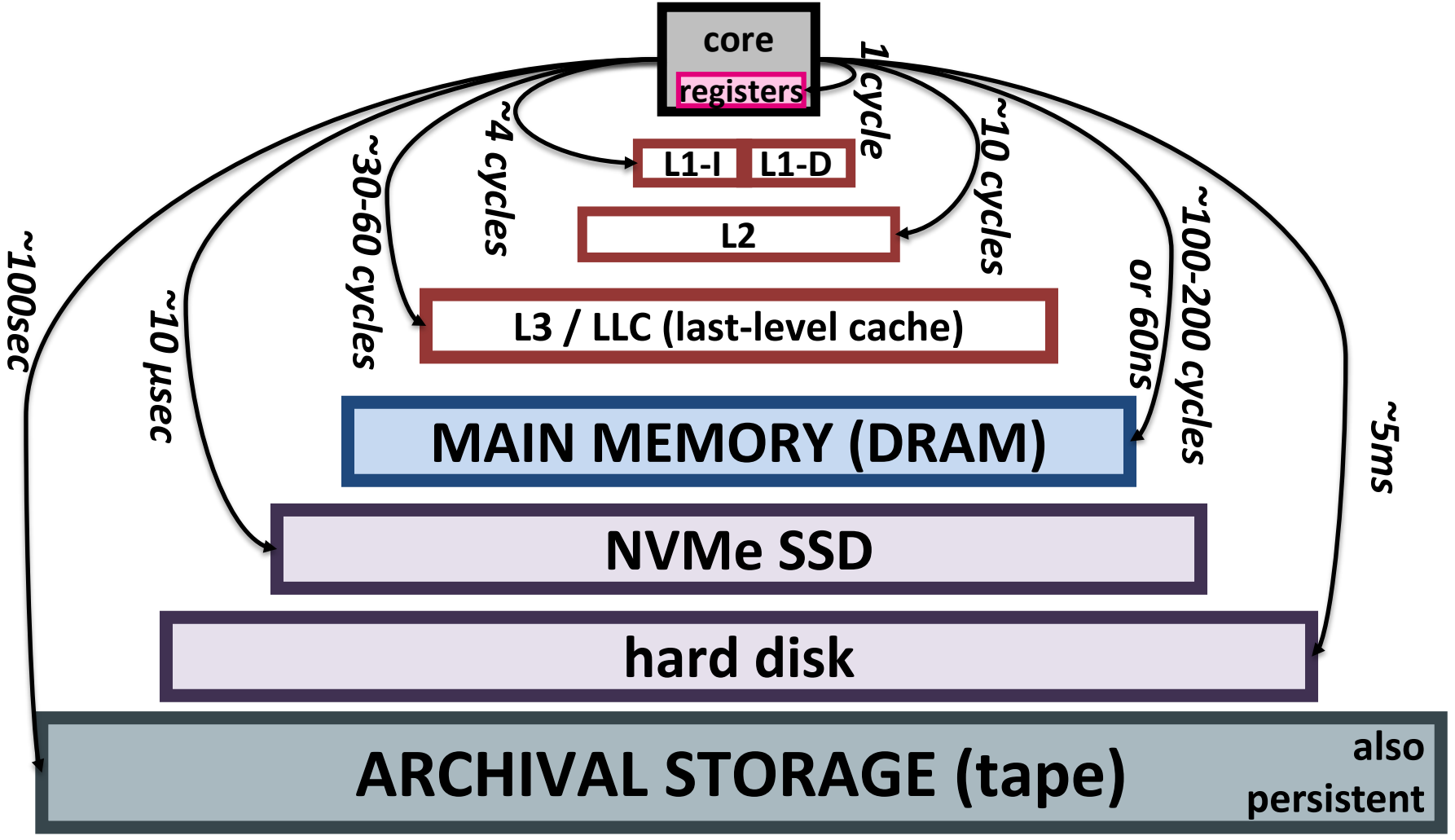
instruction & data parallelism
hardware does this automatically



multithreading
threads share
execution cycles
on the same core

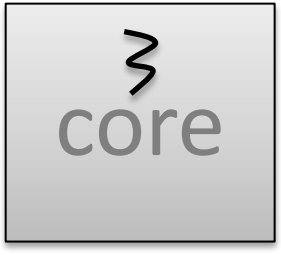
why do we need this?

single-core – access latency to storage

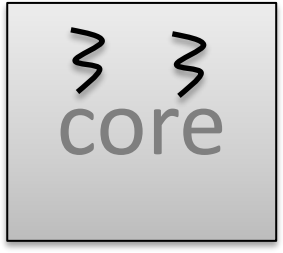


types of hardware parallelism

implicit/vertical parallelism



instruction & data parallelism
hardware does this automatically

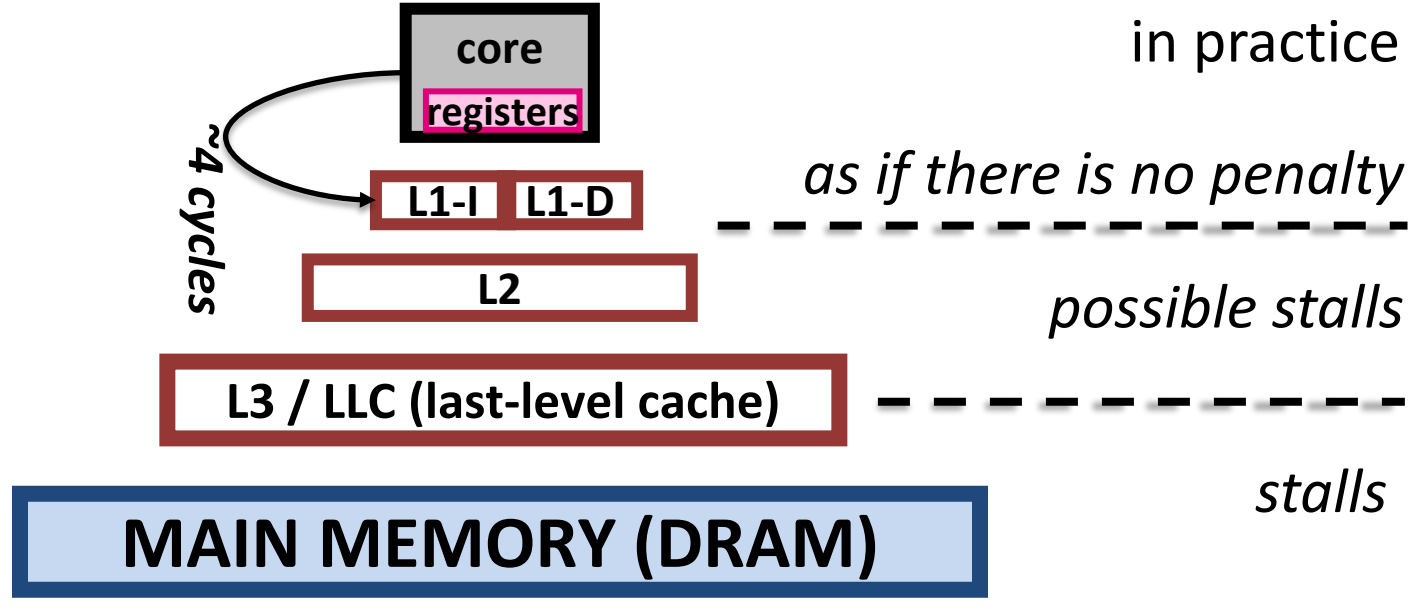


multithreading
threads share
execution cycles
on the same core

why?
we don't want cores to stay idle waiting for instruction/data accesses!

goal: minimize stall time due to cache/memory accesses
overlapping access latency for one item with other work

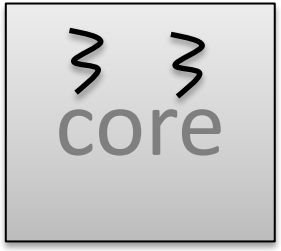
single-core – access latency to storage



stalls = 😴

types of hardware parallelism

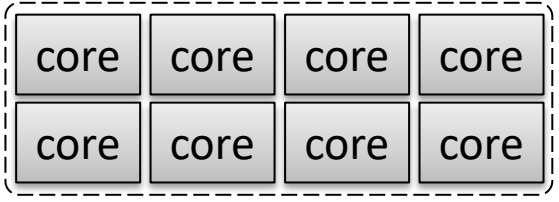
implicit/vertical parallelism ⟷ **explicit/horizontal parallelism**



single-core

instruction & data parallelism

simultaneous multithreading



multicores

multiple threads run in parallel on different cores

why do we have this?

wording courtesy of Wikipedia

for Moore's law to be practical you need Dennard scaling!

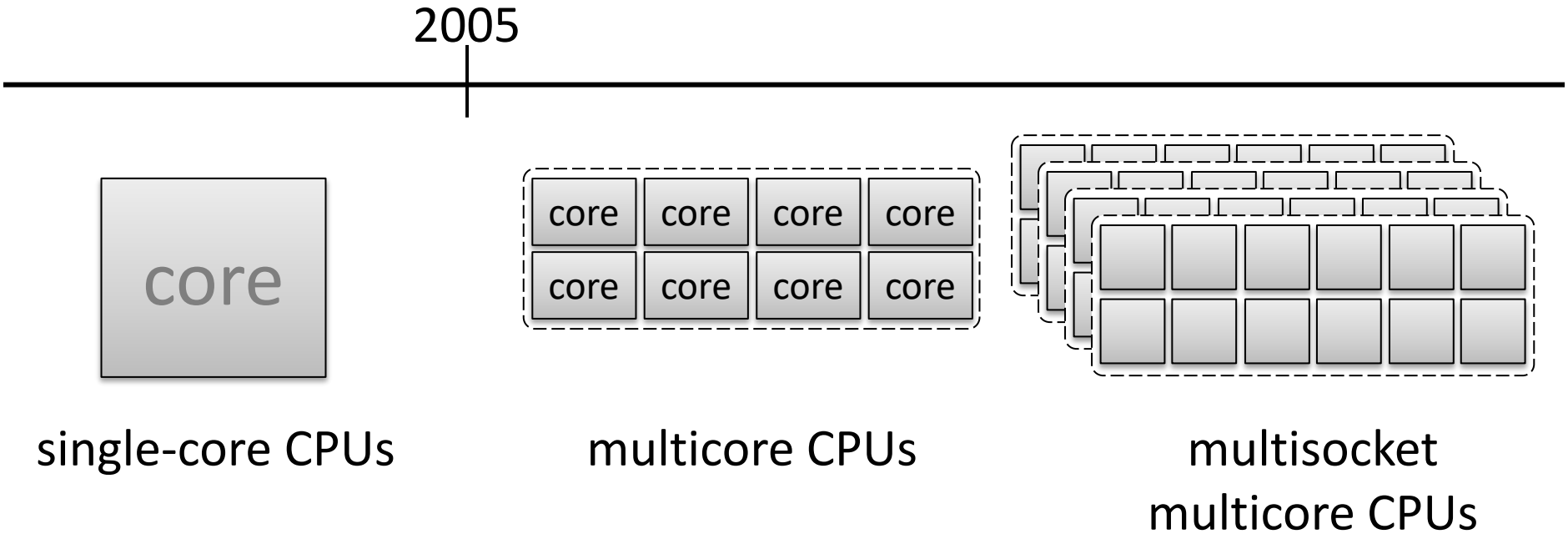
Moore's law

"… the observation that the number of transistors in a dense integrated circuit doubles approximately every two years."

Dennard scaling

" … as transistors get smaller their power density stays constant, so that the power use stays in proportion with area: both voltage and current scale (downward) with length."

commodity CPU evolution



single-core CPUs

multicore CPUs

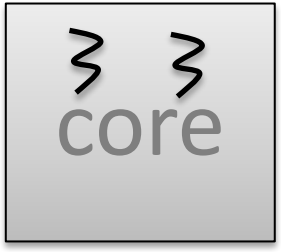
multisocket multicore CPUs

Dennard scaling doesn't hold anymore

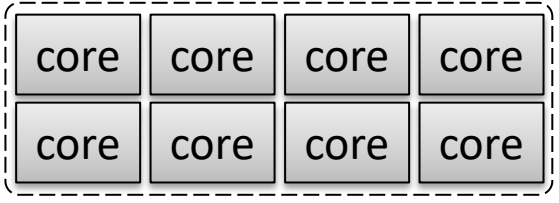
switching to multicores kept Moore's Law alive

types of hardware parallelism

implicit/vertical parallelism ⟷ **explicit/horizontal parallelism**



single-core
instruction & data parallelism
simultaneous multithreading



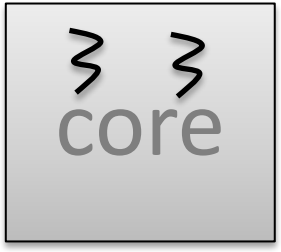
multicores
multiple threads run in
parallel on different cores

implicit parallelism → (almost) free lunch

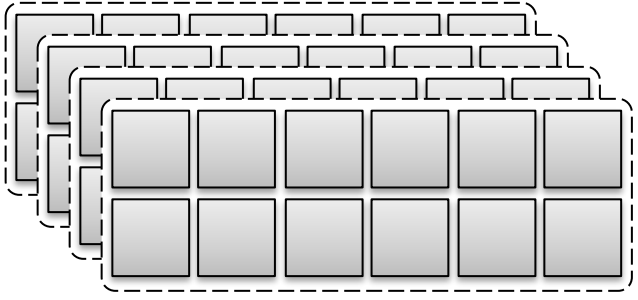
explicit parallelism → must work hard to exploit it

types of hardware parallelism

implicit/vertical parallelism ⟷ **explicit/horizontal parallelism**



single-core
instruction & data parallelism
simultaneous multithreading



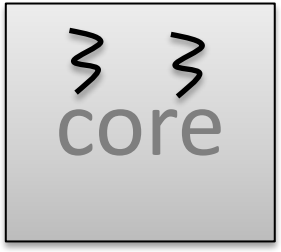
multisocket multicores
multiple processors/CPUs
in one machine

implicit parallelism → (almost) free lunch

explicit parallelism → must work hard to exploit it

types of hardware parallelism

implicit/vertical parallelism ⟷ **explicit/horizontal parallelism**



single-core
instruction & data parallelism
simultaneous multithreading

distributed systems
running a program over
multiple machines

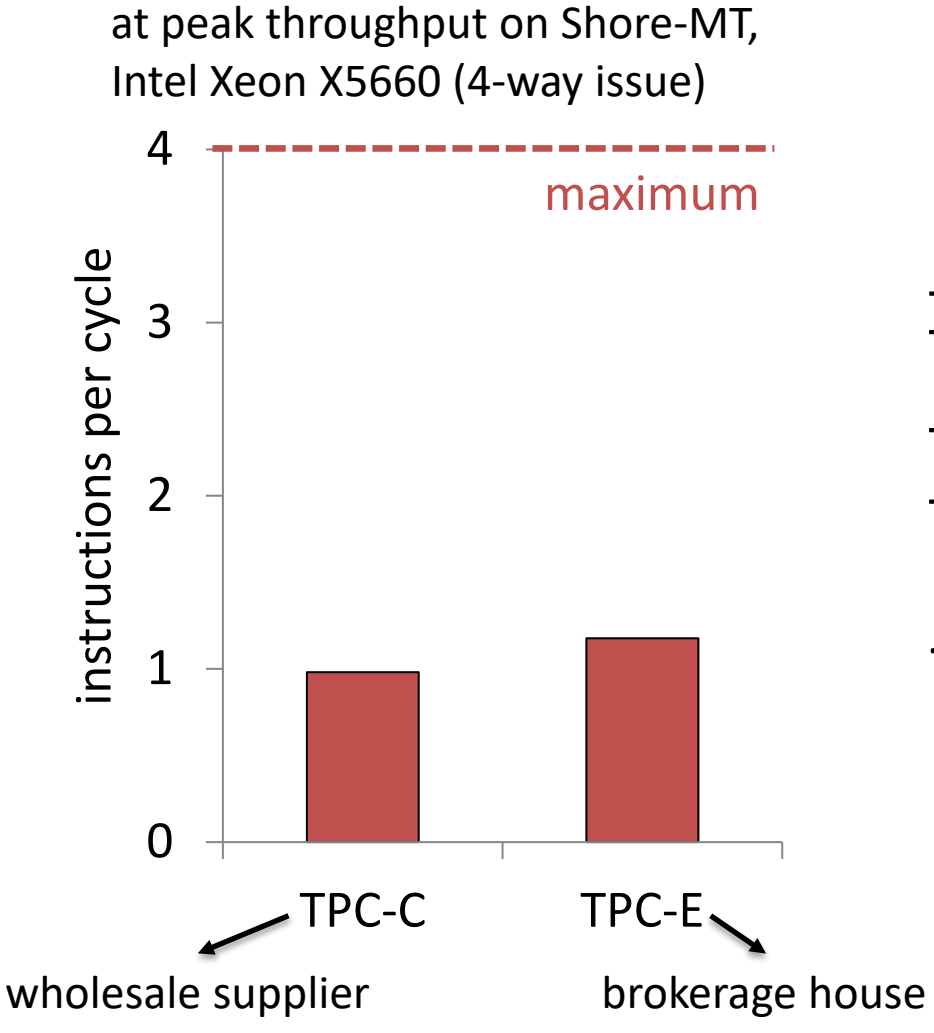
implicit parallelism → (almost) free lunch

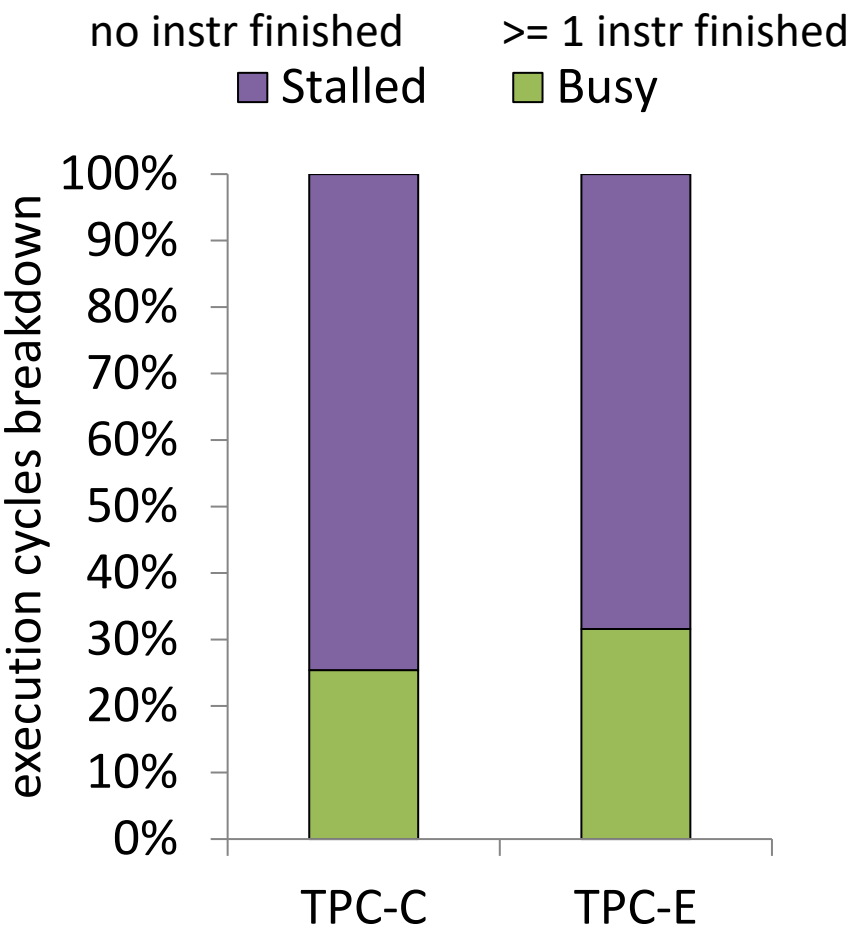
explicit parallelism → must work hard to exploit it

agenda

- types of hardware parallelism
- **OLTP & implicit parallelism**
- OLTP & explicit parallelism

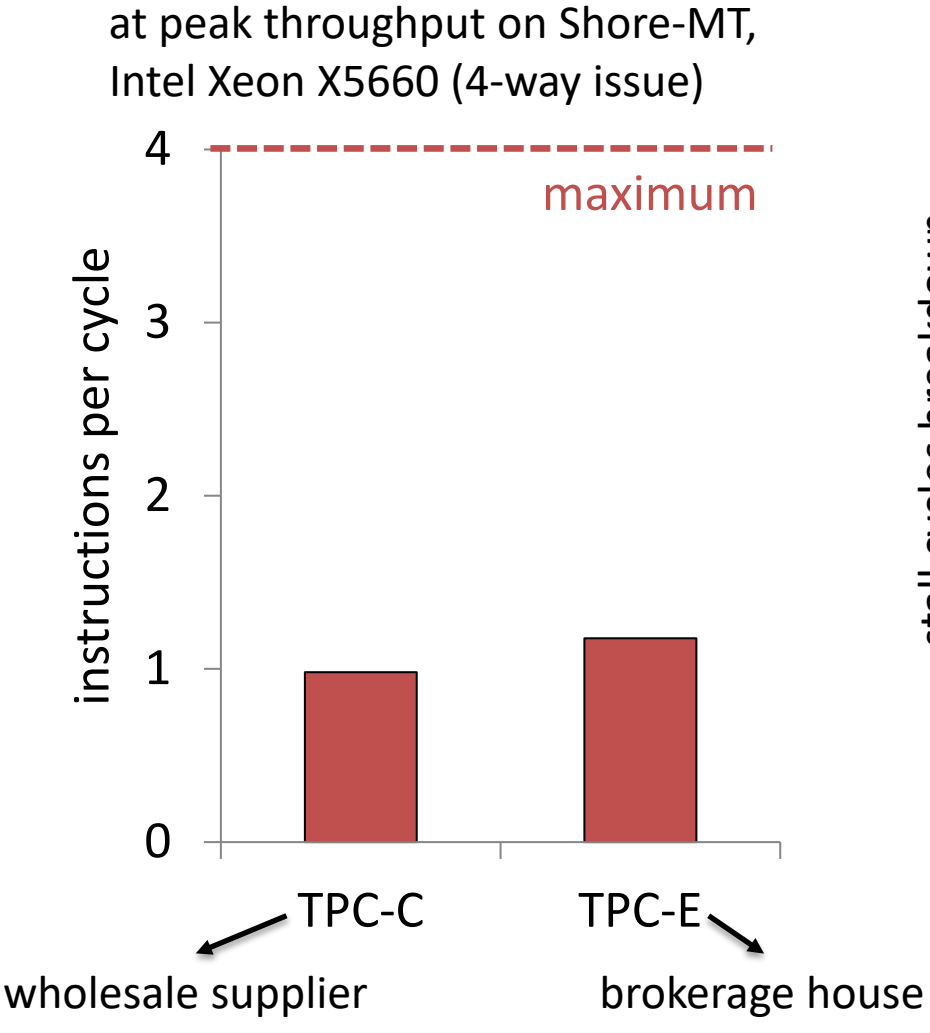
OLTP & implicit parallelism

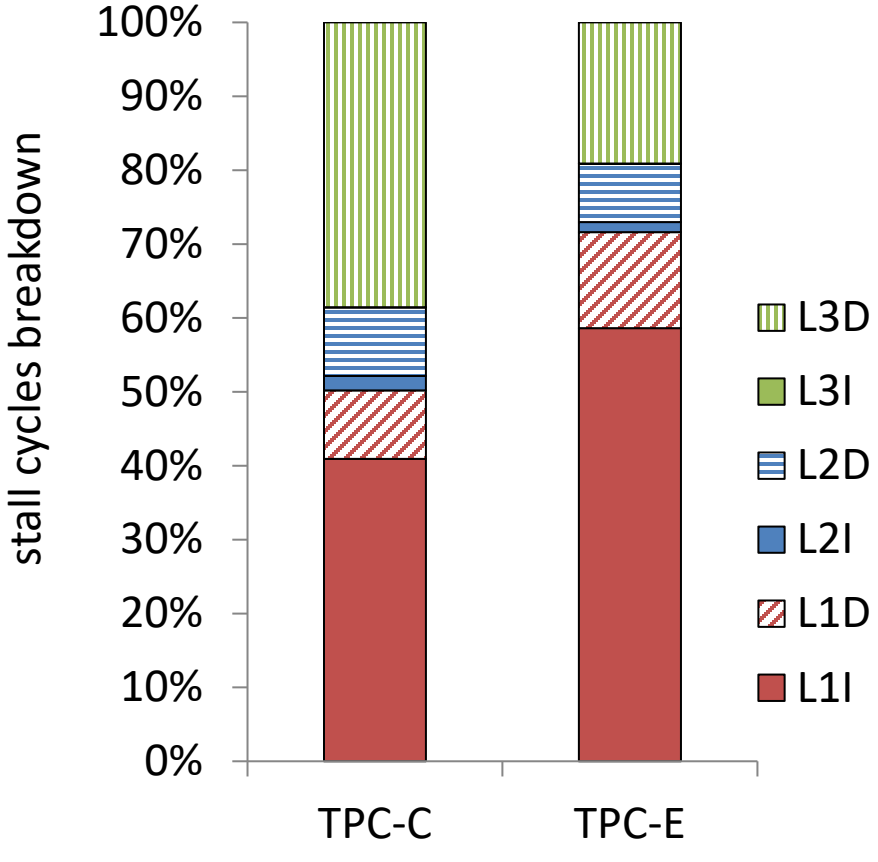




[EDBT13]

OLTP & implicit parallelism

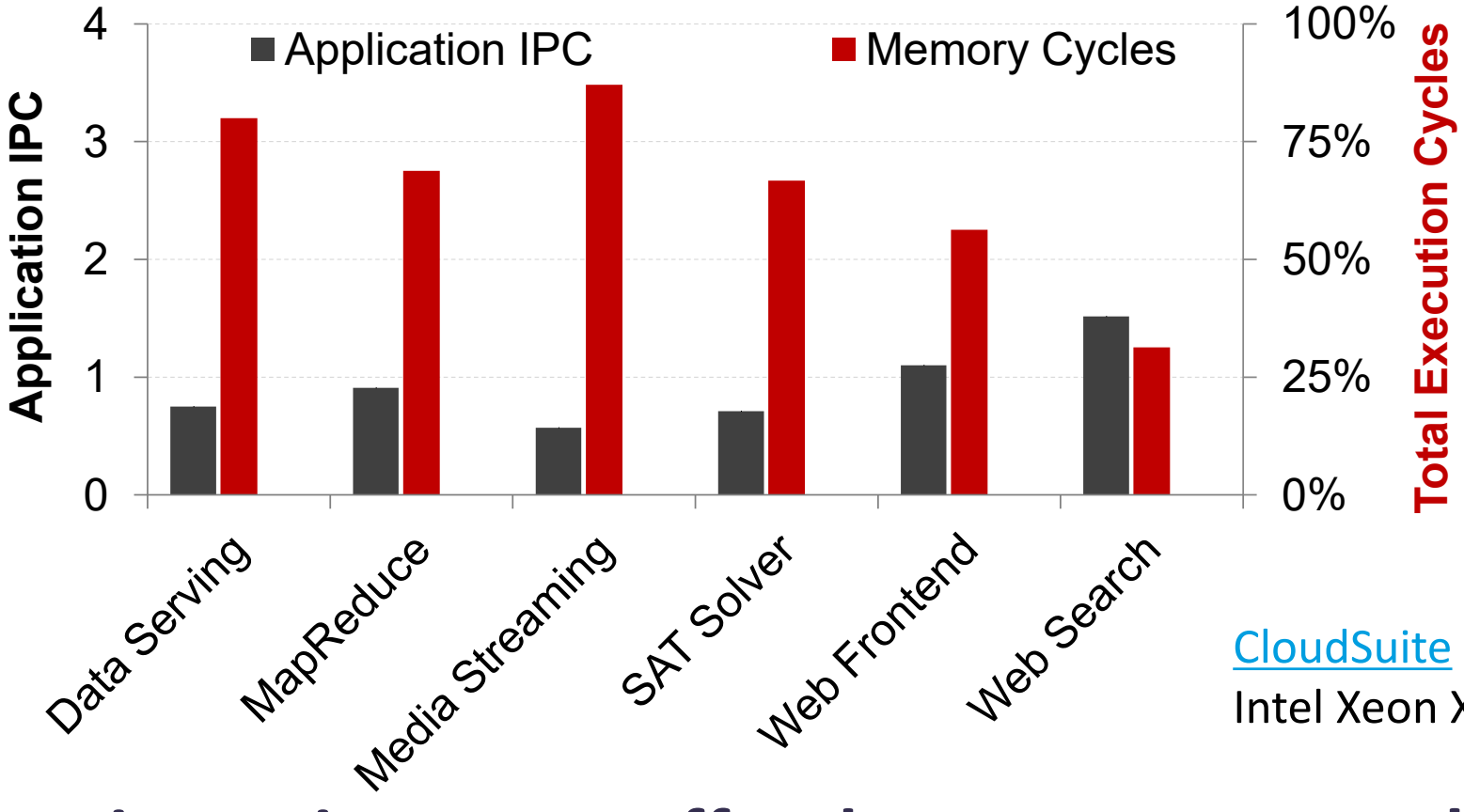




[EDBT13, DaMoN13]

memory stalls in data-intensive apps

[ASPLOS12]



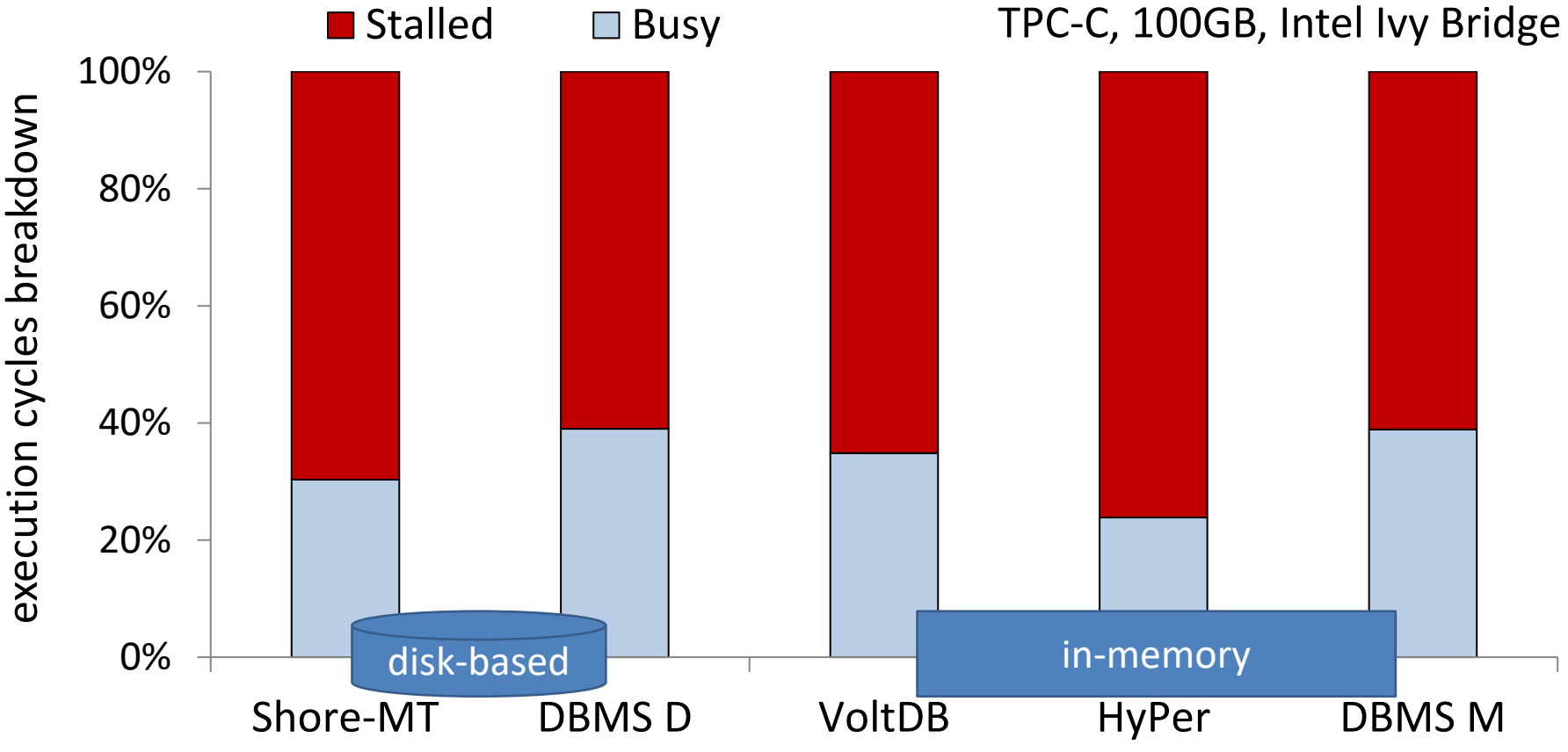
CloudSuite on Intel Xeon X5670

data-intensive apps suffer due to memory stalls

not just due to data but also instructions

what about in-memory OLTP?

[SIGMOD16]



doesn't mean these systems are bad

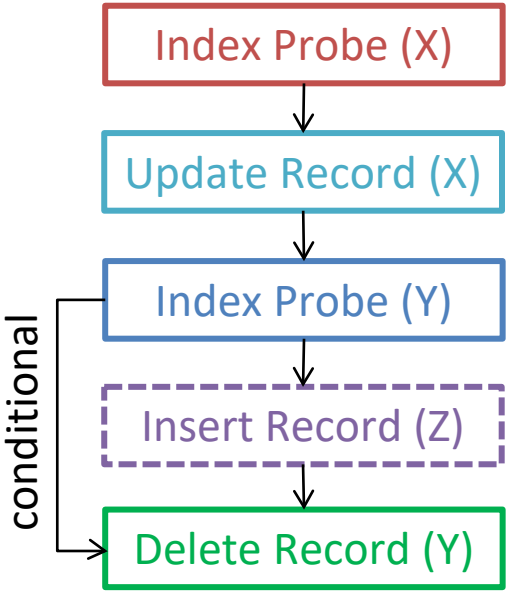
but we have room to do better

transactions under microscope

database operations

- Index Probe
- Index Scan
- Update Record
- Delete Record
- Insert Record

transaction



instances

T1

- Index Probe (X1)
- Update Record (X1)
- Index Probe (Y1)
- Delete Record(Y1)

T2

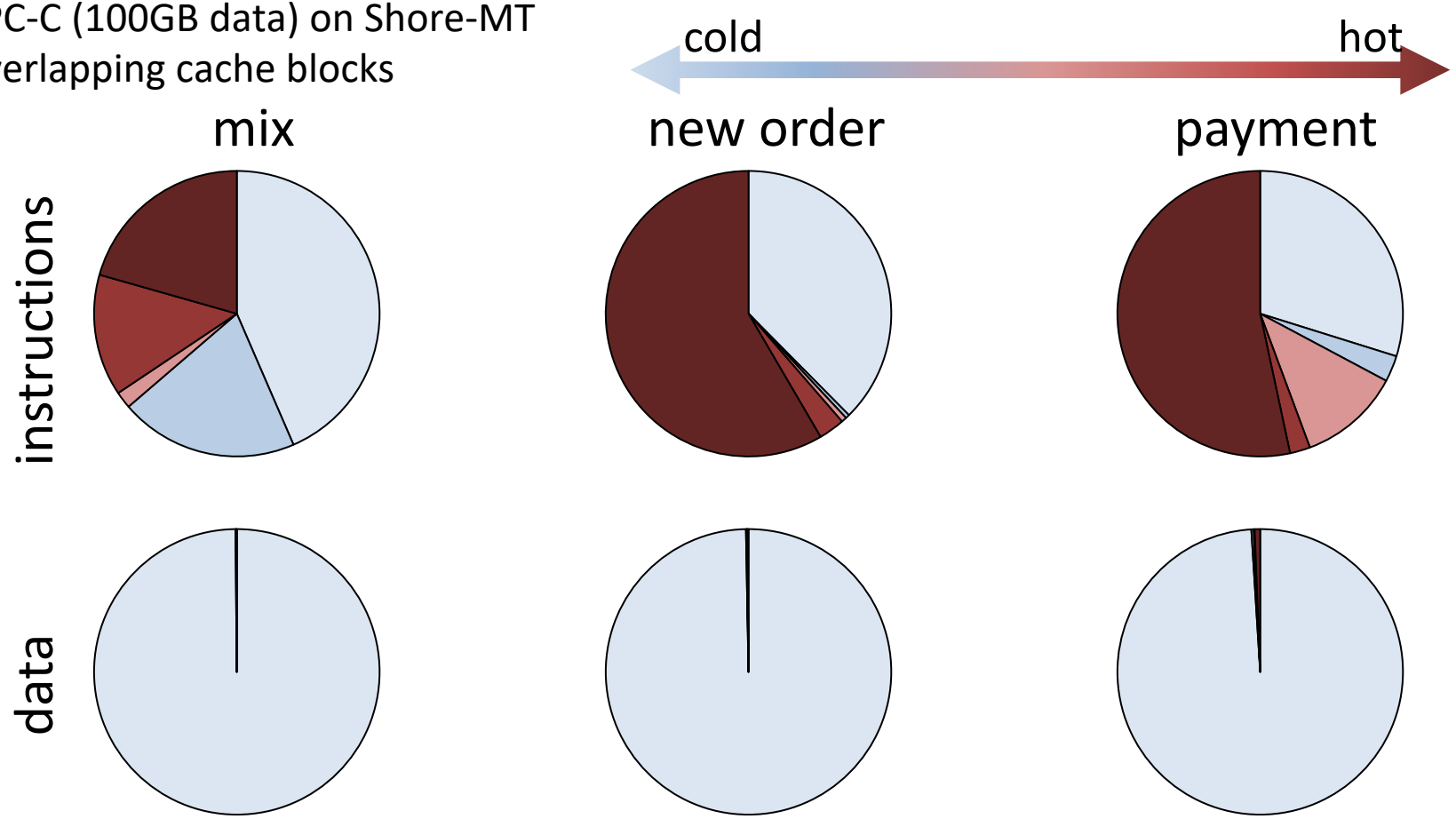
- Index Probe (X2)
- Update Record (X2)
- Index Probe (Y2)
- Insert Record(Z2)
- Delete Record(Y2)

many transactions are composed of common instructions

instruction & data overlap

[PVLDB14]

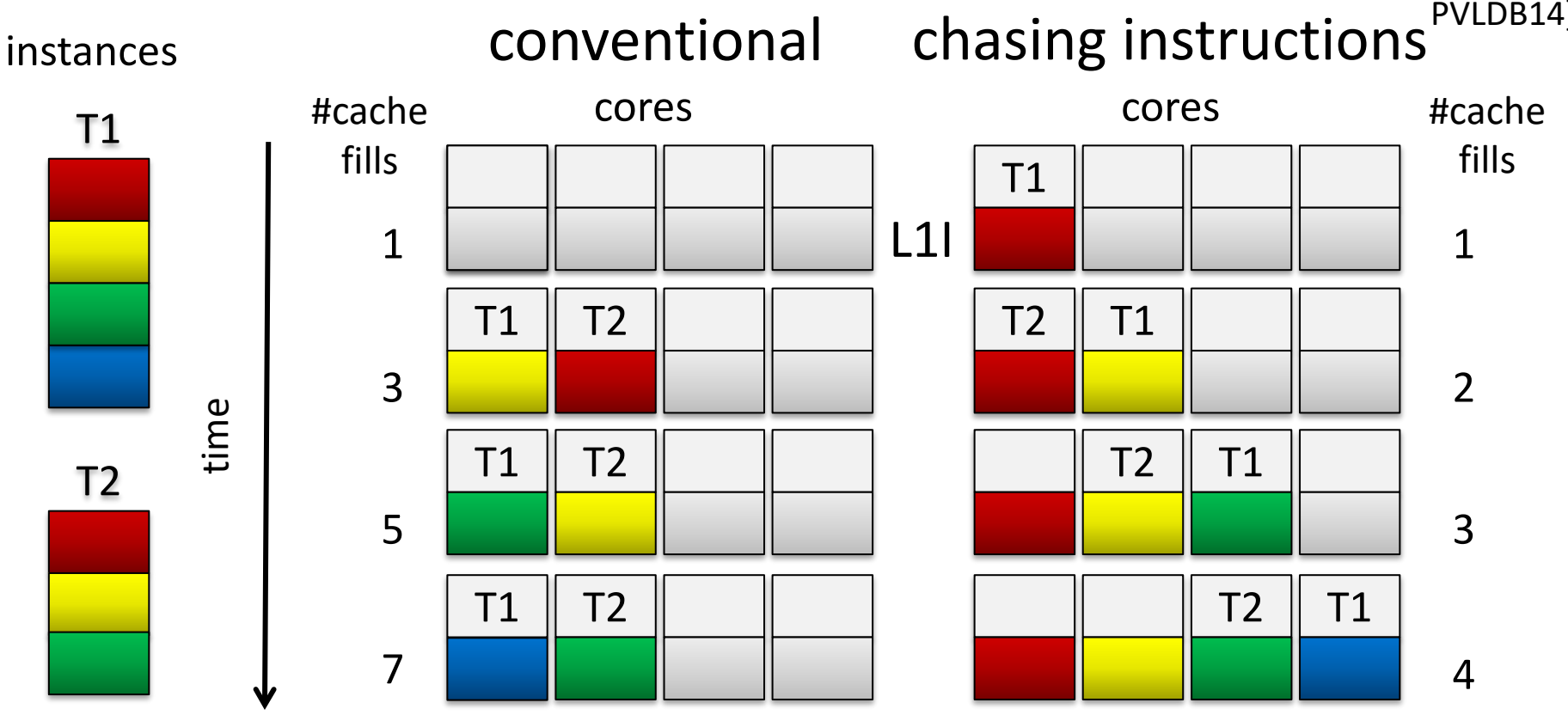
TPC-C (100GB data) on Shore-MT
overlapping cache blocks



high for instructions, low for data

utilizing instruction commonality

[MICRO12, ISCA13, PVLDB14]



can be software/hardware managed

up to 2X throughput of conventional on TPC-B/C/E

summary: OLTP & implicit parallelism

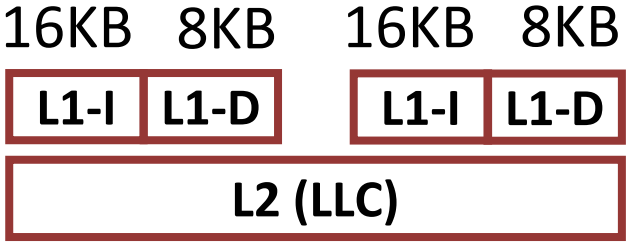
- implicit parallelism isn't completely free lunch
- > 50% of cycles are stalls for traditional OLTP
  - L1-I misses are significant
- invest in
  - utilizing instruction overlap across transactions & aggregate L1-I cache capacity
  - simplified code, cache-friendly data/code layouts, smarter query compilation …

interlude: SUN SPARC

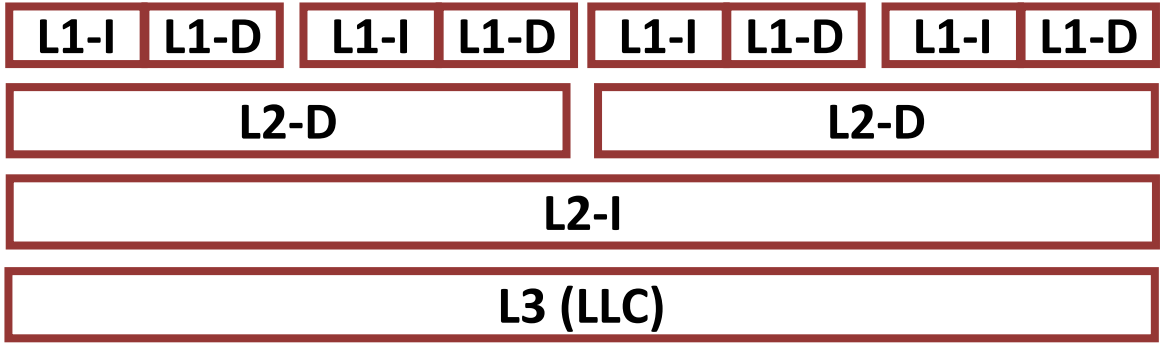
OLTP instructions have

1. **large footprint**
2. **high overlap**

UltraSPARC T2 (Niagara 2) 2007



SPARC M7 & M8



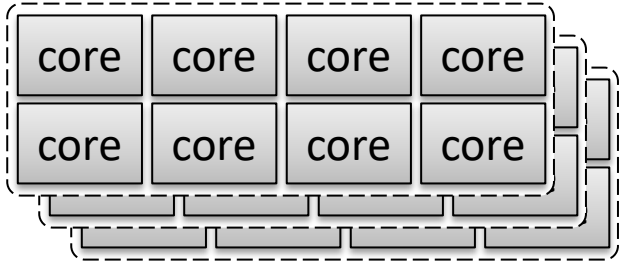
2017

agenda

- types of hardware parallelism
- OLTP & implicit parallelism
- **OLTP & explicit parallelism**

scaling-up vs scaling-out

scaling-up



adding more cores in a single server should give proportional performance increase

scaling-out

adding more servers in a data center should give proportional performance increase

for regular folk!

scaling-up vs scaling-out

scaling-up

adding more servers in a data center should give proportional performance increase

scaling-out

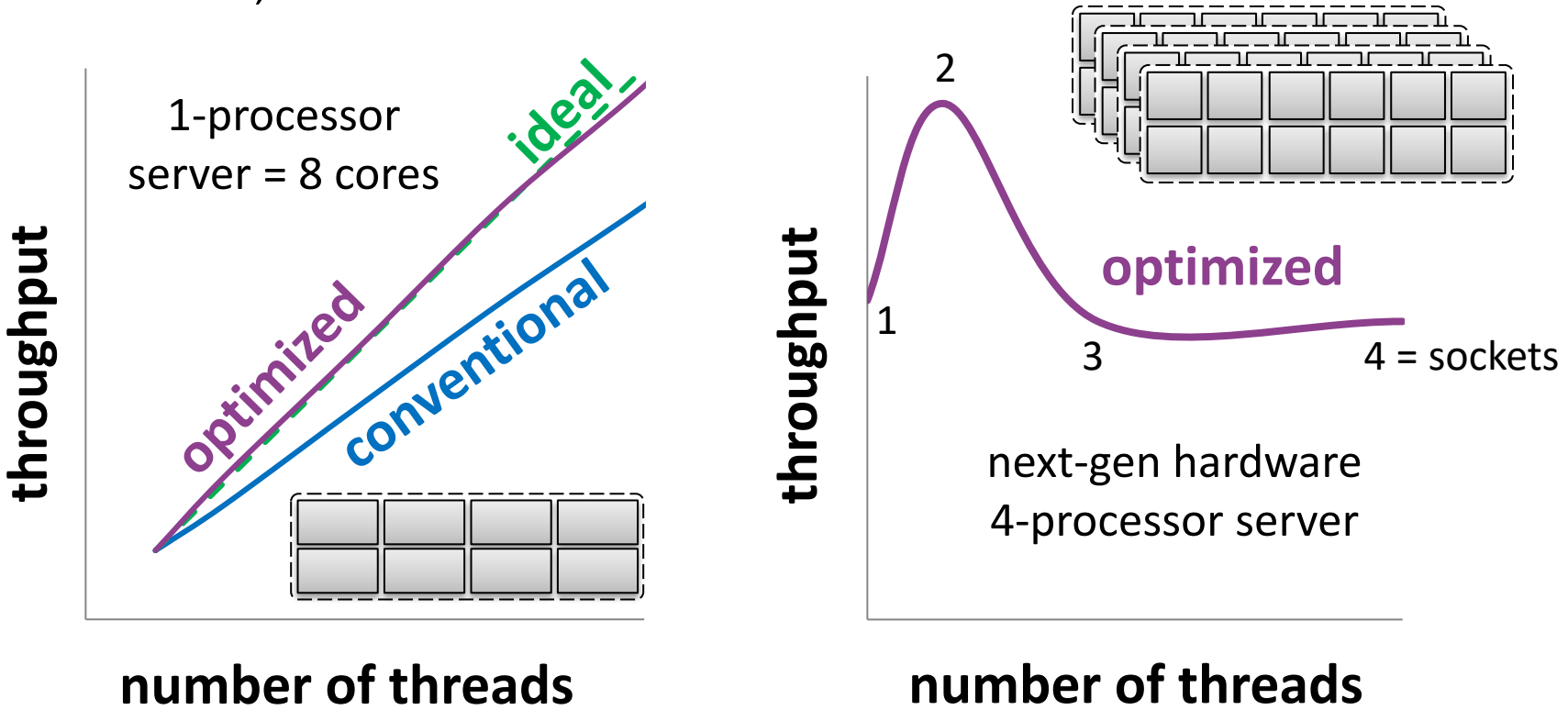
adding more data centers should give proportional performance increase

for google, amazon …!

scaling-up

[PVLDB11, PVLDB12, ICDE14]

probe one customer, read balance on Shore-MT

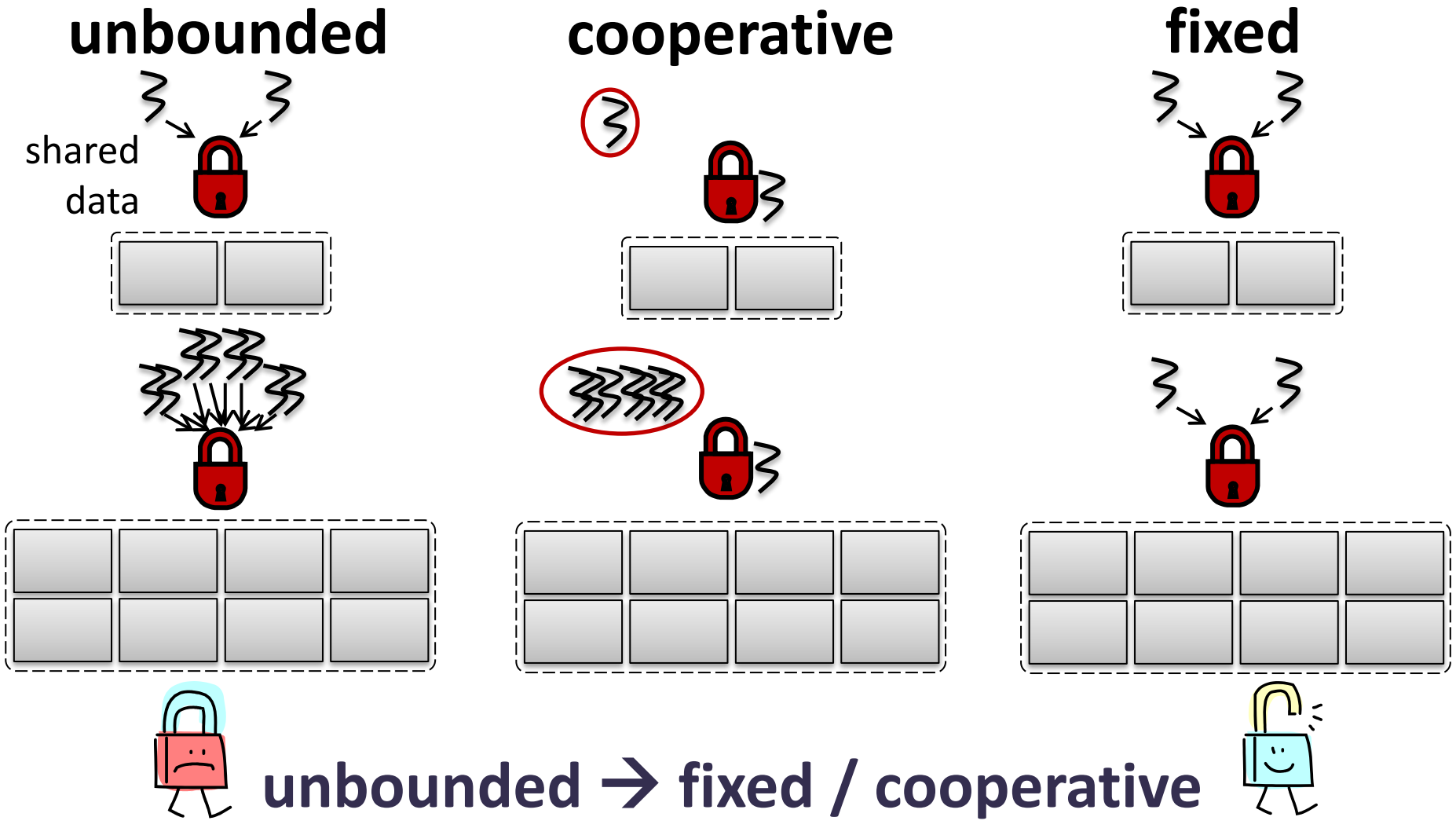


need better metrics to reason about scalability

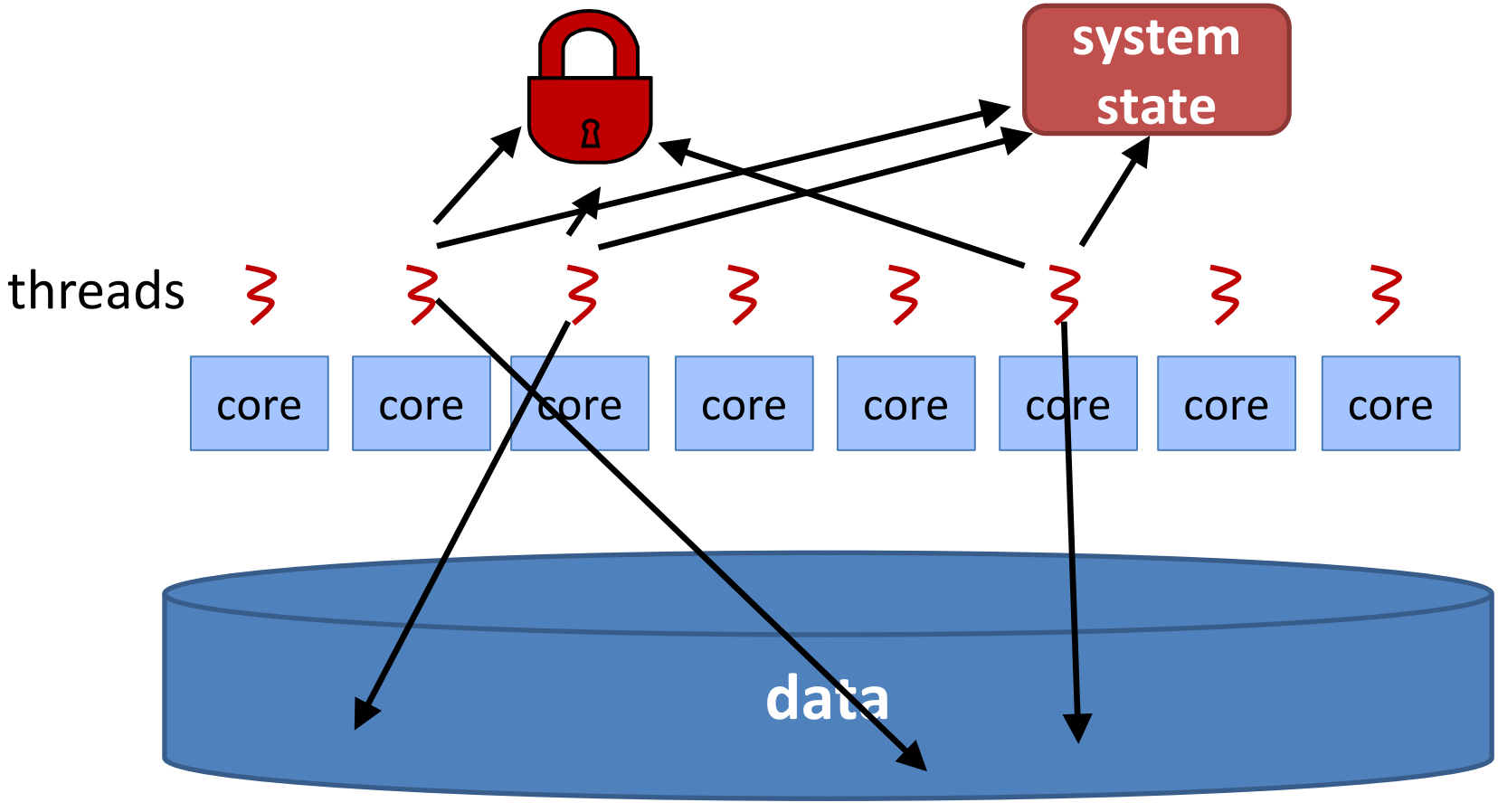
throughput measurements are not enough

critical sections / synchronization

[PVLDB11]

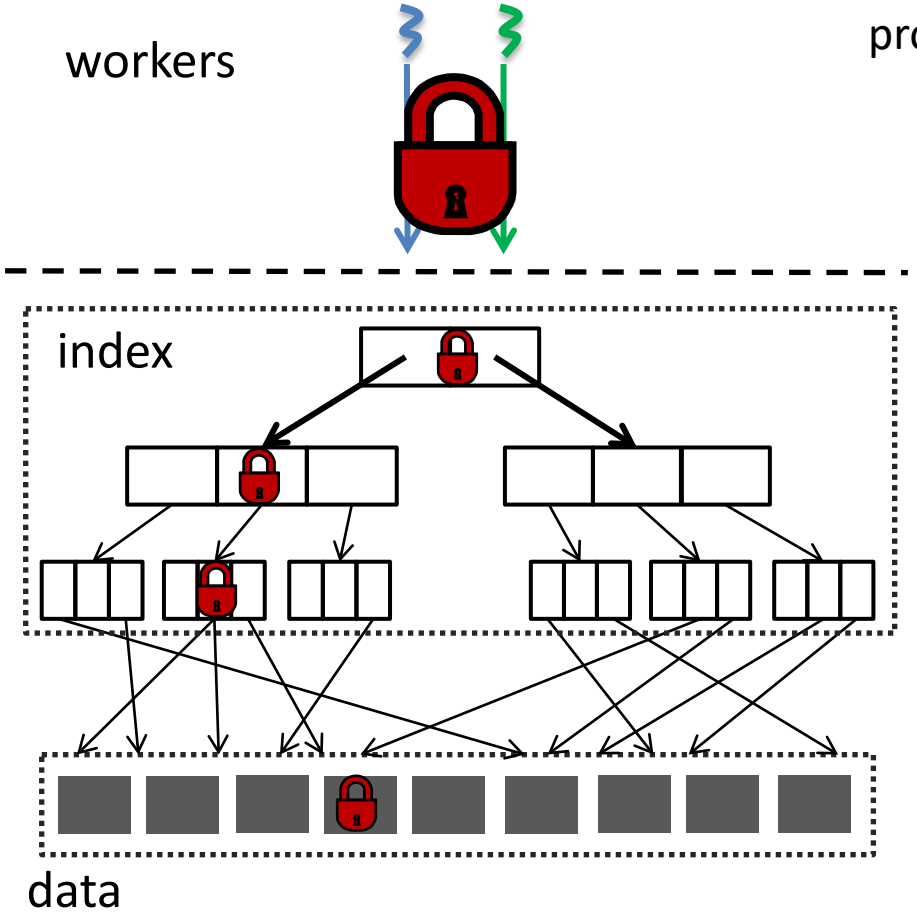


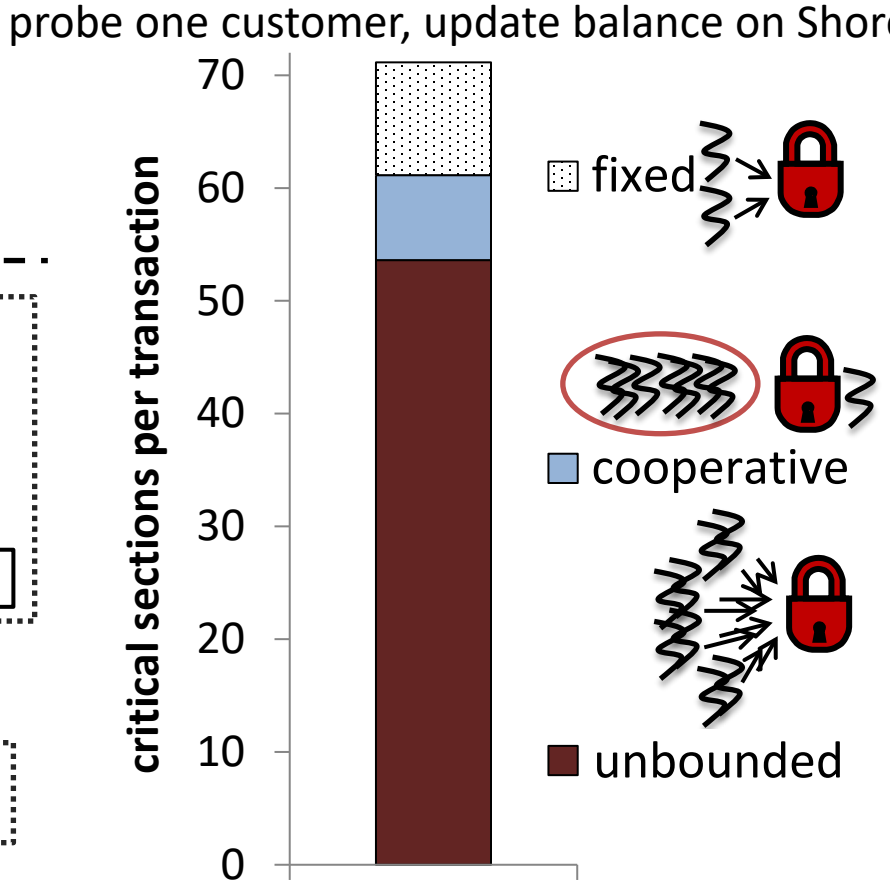
critical path of transaction execution



many unpredictable accesses to shared data

impact of unpredictable data accesses

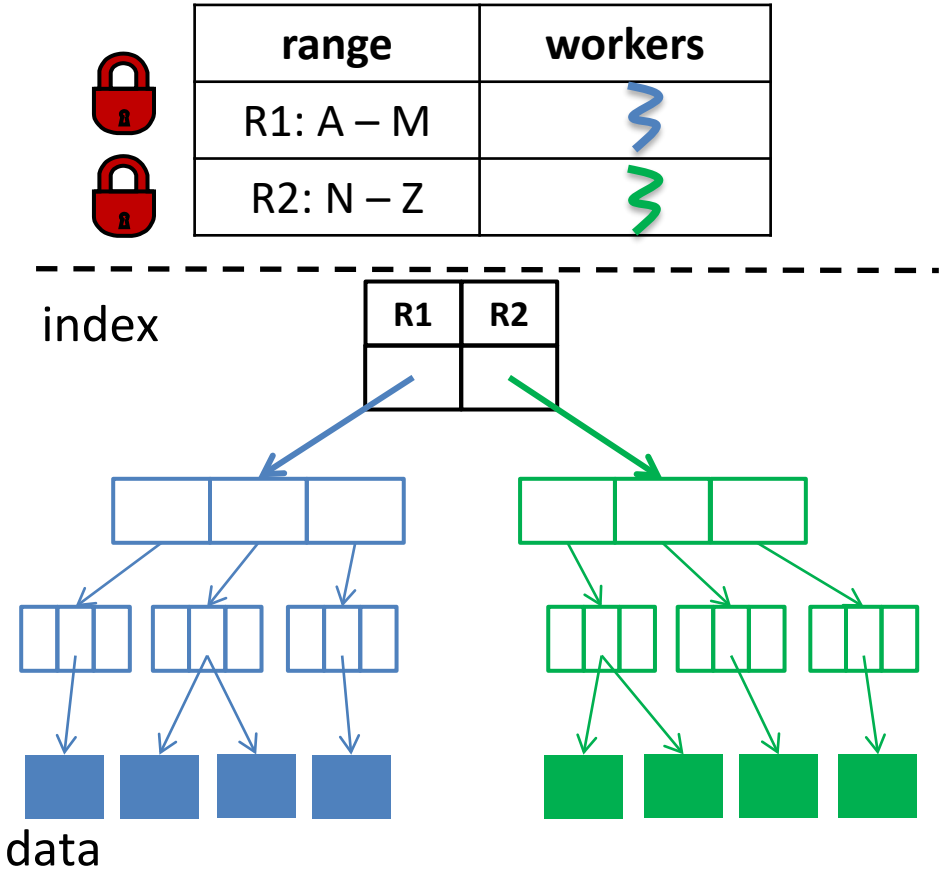


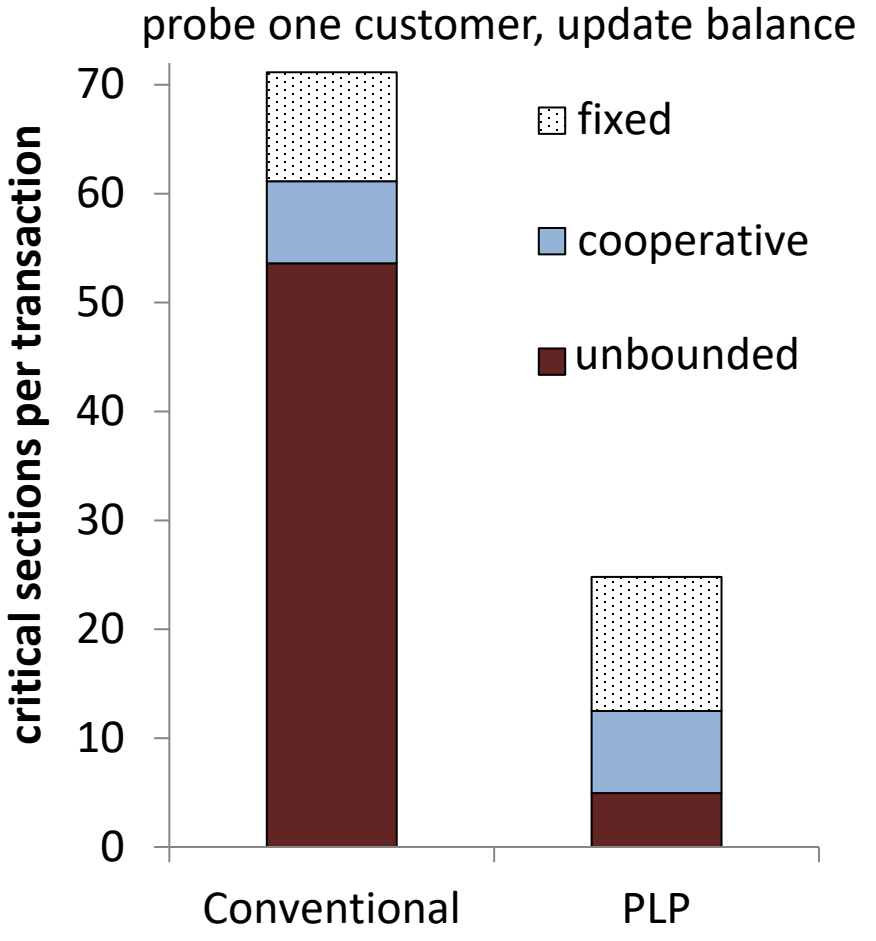


75% of critical sections are unbounded

physiological partitioning (PLP)

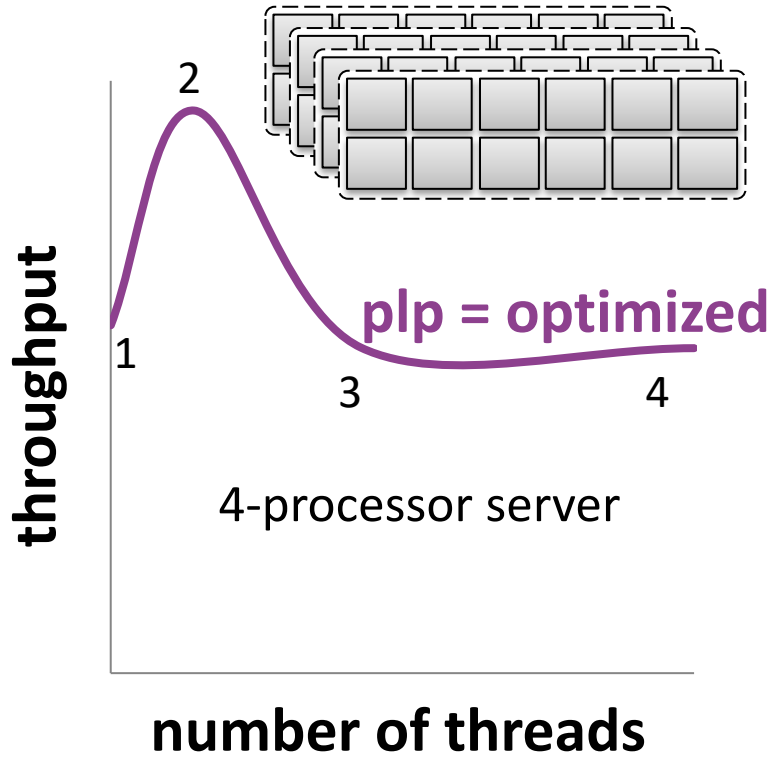
[PVLDB11]

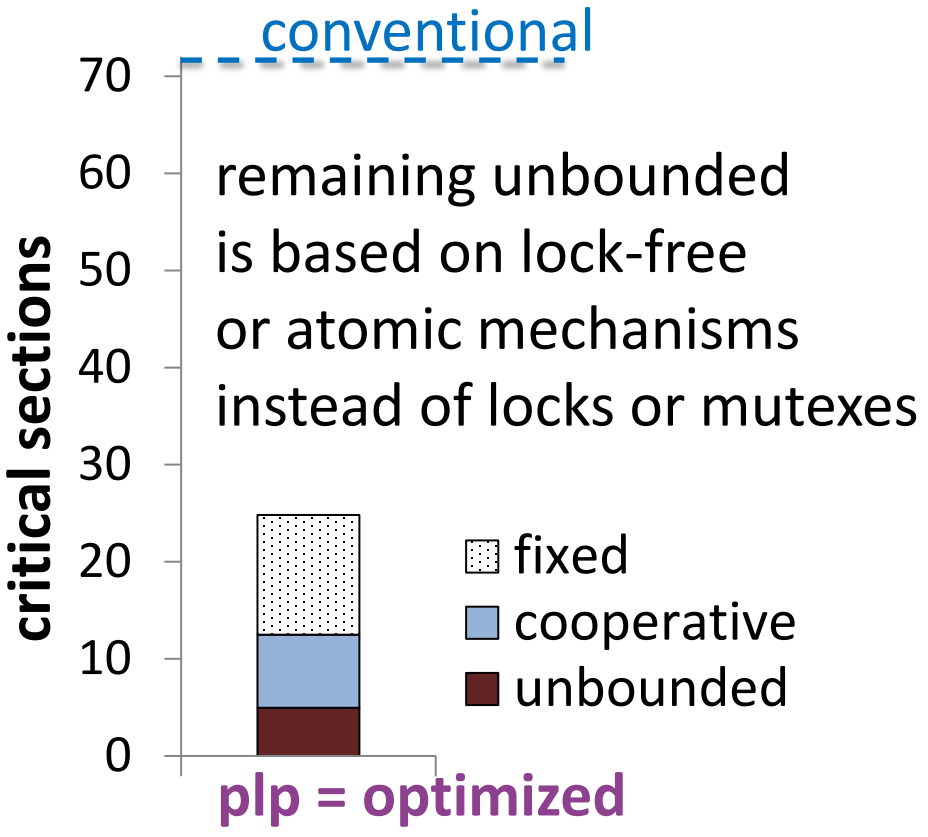




PLP eliminates 70% of critical sections

critical sections as a metric?

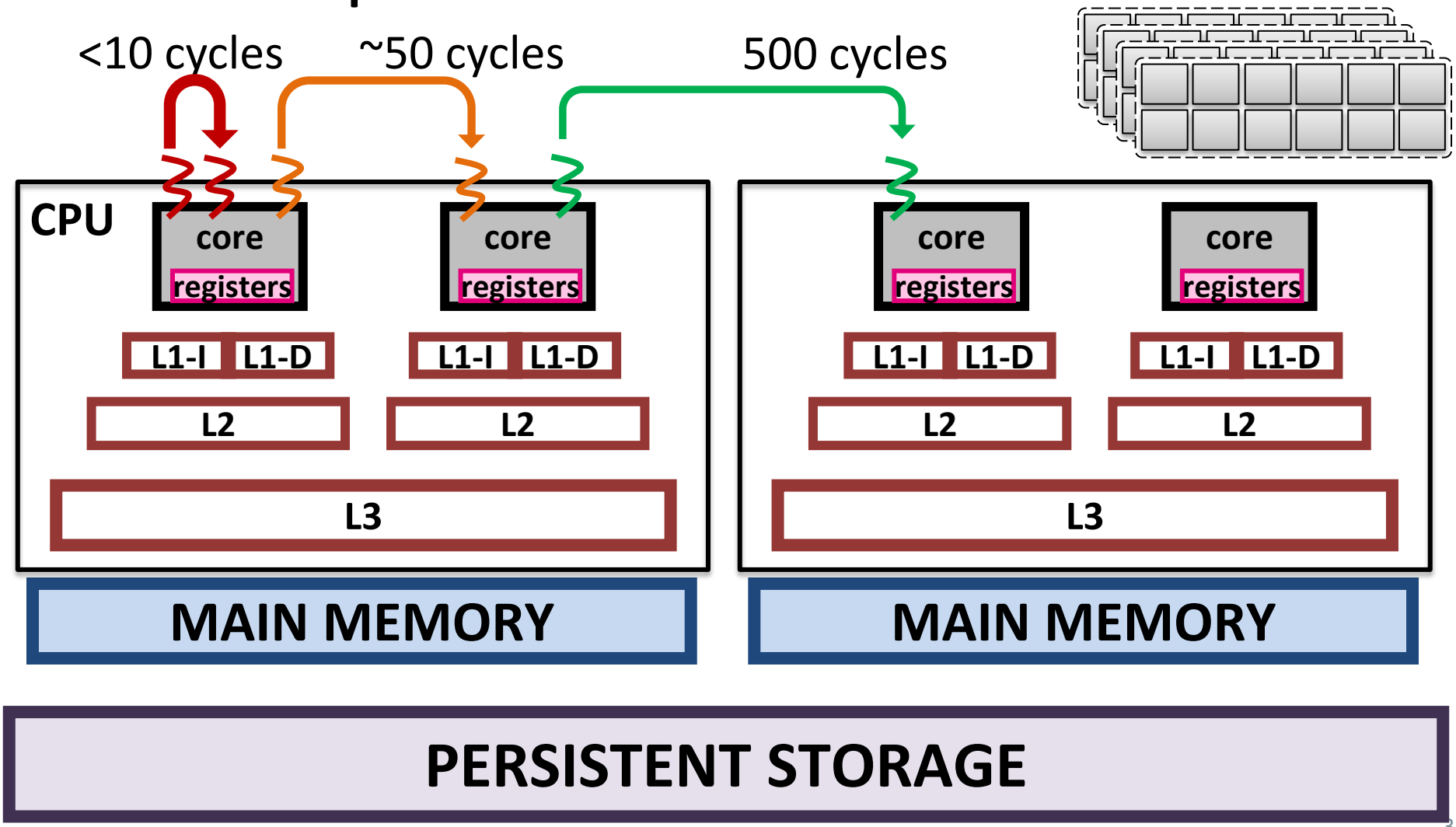




unbounded communication will hit you eventually

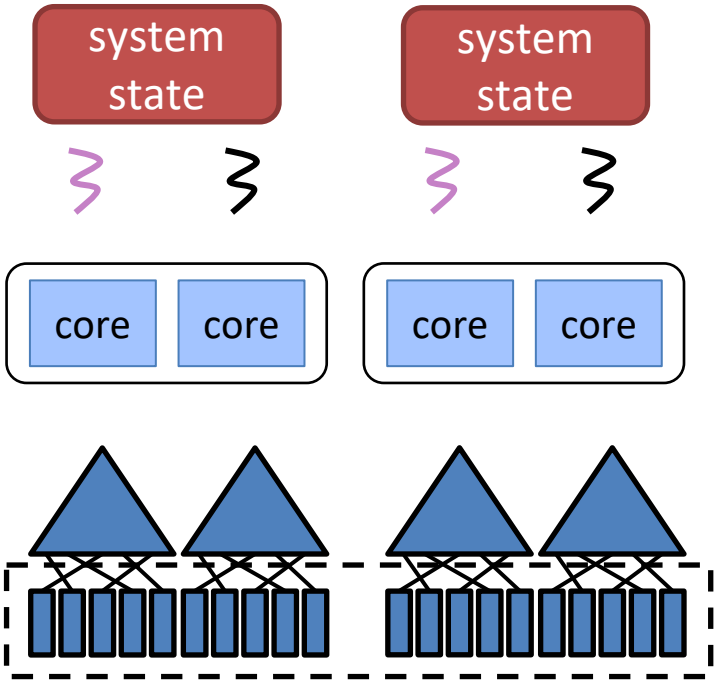
with NUMA even fixed/cooperative have issues

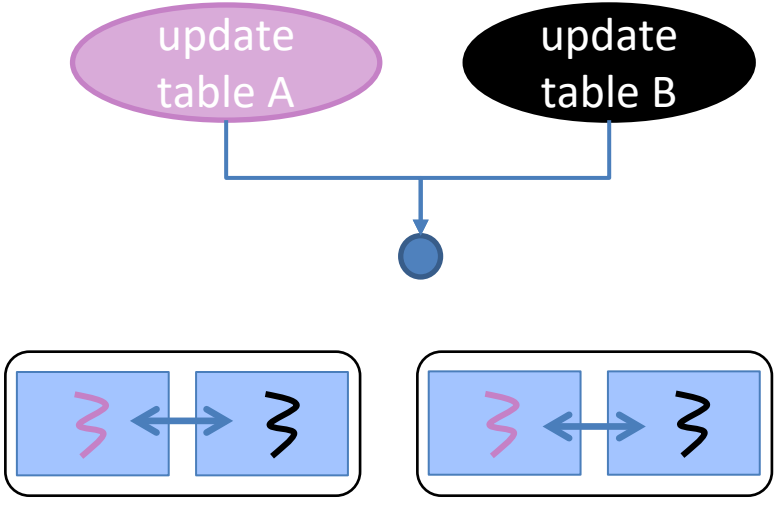
NUMA impact


<10 cycles
~50 cycles
500 cycles
CPU
core
registers
core
registers
core
registers
core
registers
L1-I
L1-D
L1-I
L1-D
L1-I
L1-D
L1-I
L1-D
L2
L2
L2
L2
L3
L3
MAIN MEMORY
MAIN MEMORY
PERSISTENT STORAGE

ATraPos: NUMA-aware PLP

[ICDE14]

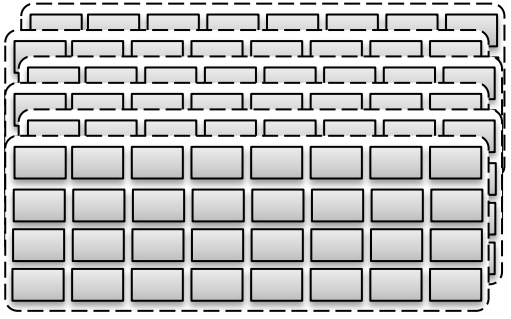




limit unbounded communication within a socket

keep access latencies predictable

summary: OLTP & explicit parallelism

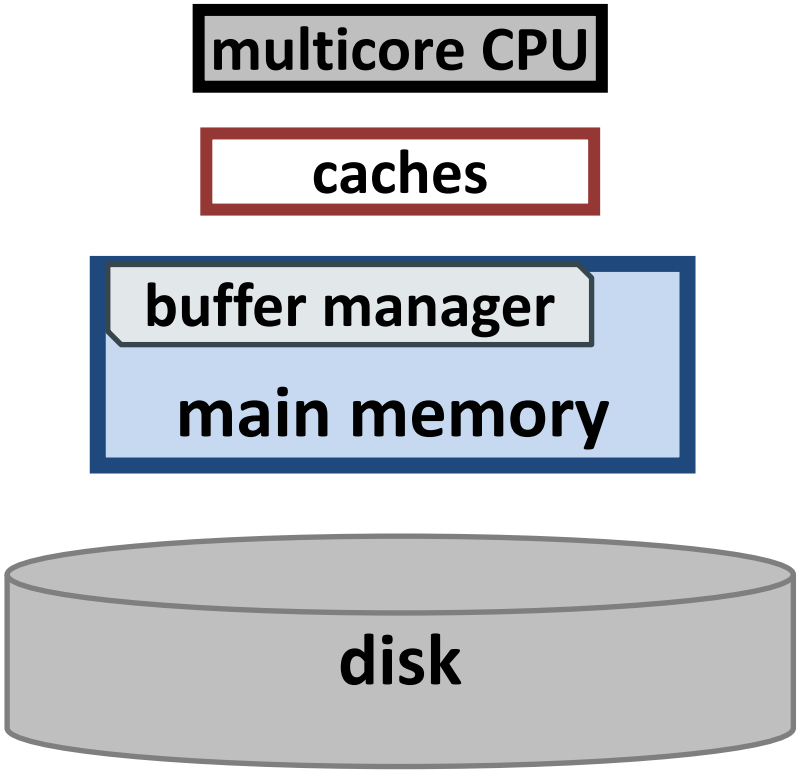


- **high throughput != scalable**
- **lock freedom != scalable**
- eliminate any unbounded communication
  - or at least bound it within a socket
- keep fixed/cooperative communication among cores with similar/predictable access latency

  → avoid sharing data across different processors (avoid NUMA impact)

today: traditional vs. modern OLTP

traditional



main-memory-optimized

- non-blocking concurrency control
- query compilation that generates more efficient code

- no / light buffer manager
- data organized for better cache accesses

- no / minimal disk use during transactions
- lightweight logging & replication for recovery
- optimize for PMem & SSDs instead

references / credits for the slides

slide 30 & 34-35 are Danica Porobic's slides from her ICDE14 talk

[ASPLOS12] M. Ferdman, A. Adileh, O. Kocberber, S. Volos, M. Alisafaee, D. Jevdjic, C. Kaynak, A. D. Popescu, A. Ailamaki, B. Falsafi. Clearing the Clouds: A Study of Emerging Scale-out Workloads on Modern Hardware.

[DaMoN13] P. Tözün, B. Gold, and A. Ailamaki: OLTP in Wonderland -- Where do cache misses come from in major OLTP components?

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