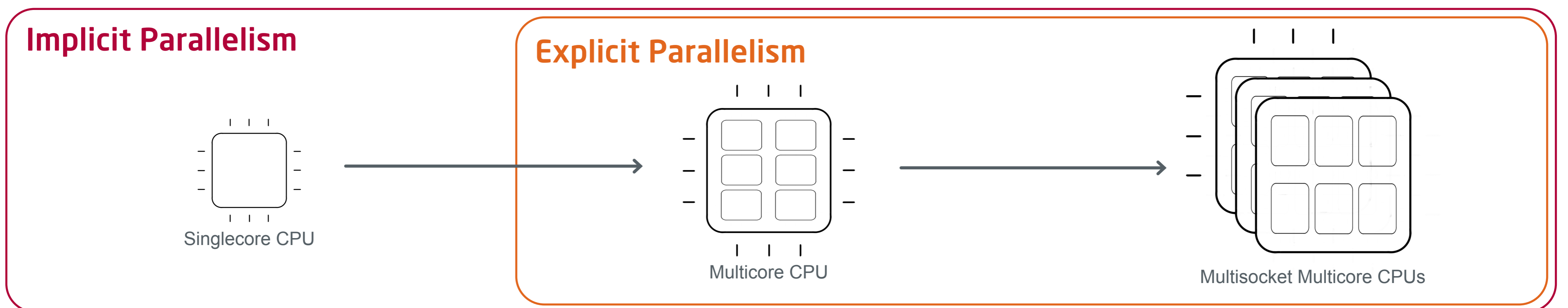


Dimensions of Hardware Parallelism and Exploiting Them for Data-Intensive Systems

CPU Evolution

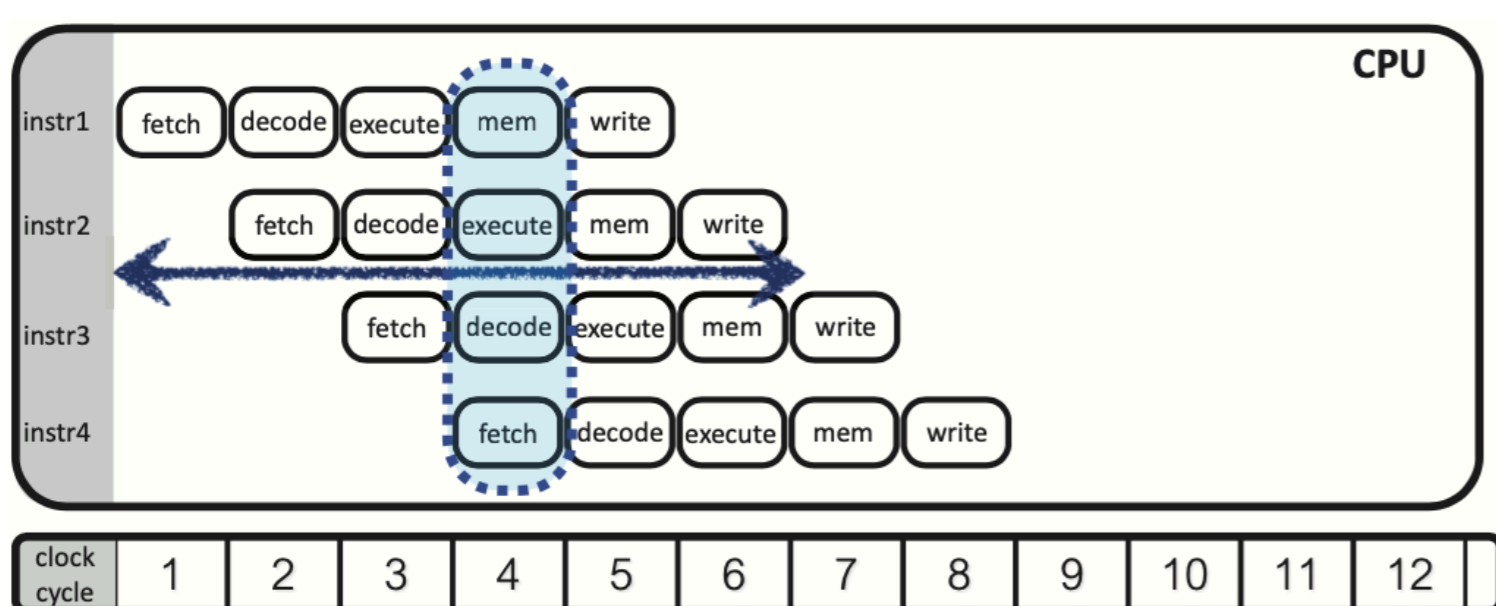


Implicit Parallelism

On single core systems there are different techniques to increase the throughput by using implicit parallelization. In most cases, this is achieved by a special hardware design.

Instruction Pipelining

Is a instruction-level parallelisation technique where instructions are scheduled, so that the individual stages overlap and every part of the processor is busy.



Out of Order Execution

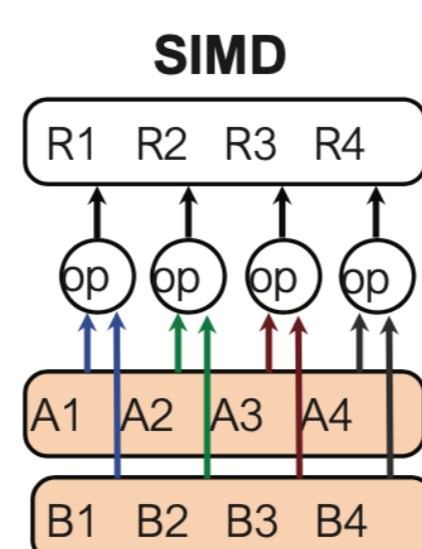
The transactions are scheduled depending on the data availability.

Simultaneous Multithreading

The registers in the core are shared, so that they do not need to be readjusted in case of a context switch.

Single-Input-Multiple-Data (SIMD)

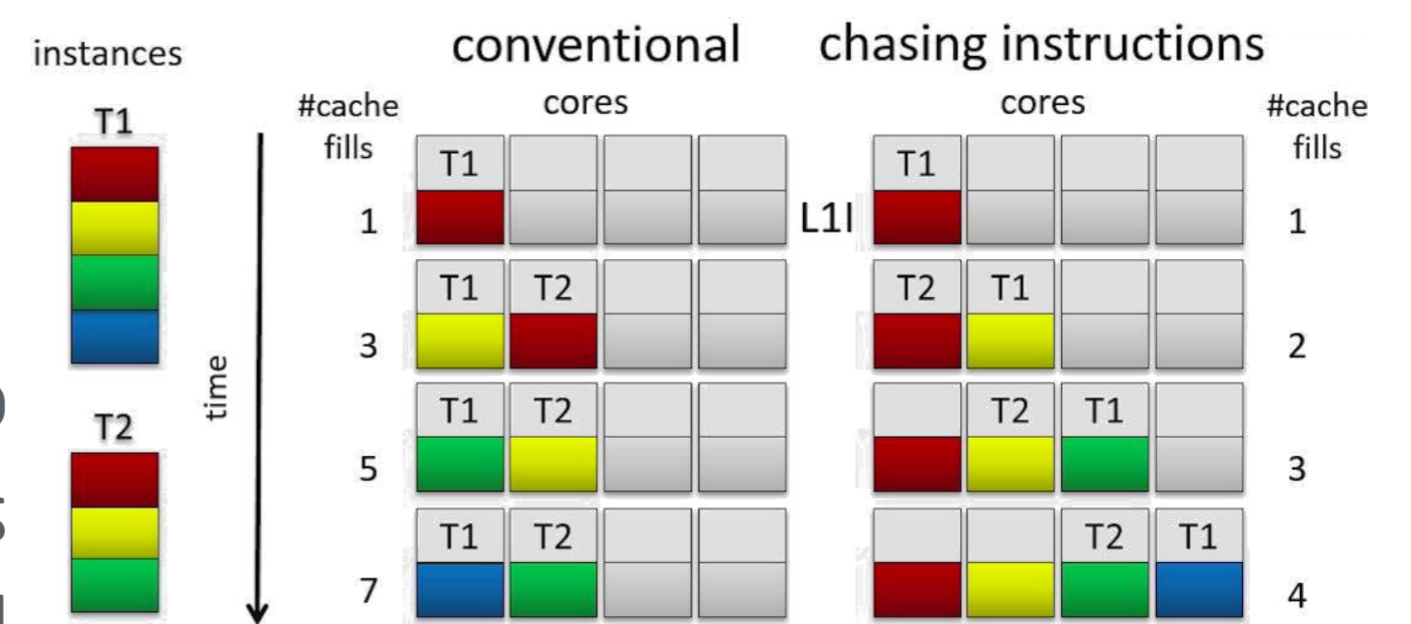
An instruction can process several data units at once due to specially adapted CPUs, this must be controlled by the software.



Explicit Parallelism

One can further improve the throughput of a multicore or multiprocessor system by exploiting explicit parallelism through software. In database applications, many transactions use the same set of instructions. Advantage of this effect can be taken by segmenting the transactions so that identical instructions are executed on the same cores, thereby reducing the need for context switching and the instruction load time.

There is also data that needs to be accessed



very often, which is a kind of bottleneck. These are also called critical sections, because not all threads can access them at the same time, and so the speed does not scale with the number of cores. If the data is well known, reducing the number of critical sections by splitting the data or using B-trees with multiple roots is possible. This so-called physiological partitioning (PLP) can reduce the critical sections by about 70%, further increasing throughput.

Project participants

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Credits

Presentation by Prof. Dr. Pinar Tözün
Databases on Modern Hardware: How to Stop Underutilization and Love Multicores