

Schriftenverzeichnis

Buchbeiträge

- A1) J. Beister, R. Wollowski: *Controller Implementation by Asynchronous Sequential Circuits Generated from a Petri Net Specification of Required Behaviour.* In: G. Saucier, J. Trilhe (Hrsg.): *Synthesis for Control Dominated Circuits.* IFIP Transactions A-22, Elsevier Science Publishers (1993) 103–115
- A2) R. Wollowski, J. Beister: *Comprehensive Causal Specification of Asynchronous Controller and Arbiter Behaviour.* Chapter 1 in: A. Yakovlev, L. Gomes, L. Lavagno (Hrsg.): *Hardware Design and Petri Nets.* Springer (2000) 3–32
- A3) W. Vogler, R. Wollowski: *Decomposition in asynchronous circuit design.* In: *Concurrency and Hardware Design.* Lecture Notes in Computer Science 2549, Springer (2002), 152 – 190

Begutachtete Tagungs- und Zeitschriftenbeiträge

- B1) (mit J. Beister, M. Kuhn) *High-Level Design and GAL Implementation of an Asynchronous Controller for a Daisy-Chainable VME Bus Interrupt Requester.* Proc. 3rd Int. Workshop on Field Programmable Logic and Application, Jesus College, University of Oxford, England (Sept. 1993)
- B2) (mit J. Beister) *Precise Petri Net Modelling of Critical Races in Asynchronous Arbiters and Synchronizers.* Proc. 1st Workshop Hardware Design and Petrinets (HWPN'98) within 19th International Conference on Application and Theory of Petri Nets, Lissabon (Juni 1998) 46–65
- B3) J. Beister, G. Eckstein, R. Wollowski: *From STG to Extended-Burst-Mode Machines.* 5th Int. Symposium on Advanced Research in Asynchronous Circuits and Systems, Barcelona (April 1999), IEEE, 145–158
- B4) (mit J. Beister) *Synthese asynchroner Steuerwerksverbände aus der Petrinetz-Spezifikation des Sollverhaltens – ein Überblick.* Tagungsband 6. Fachtagung Entwicklung und Betrieb komplexer Automatisierungssysteme (EKA'99), Braunschweig (Mai 1999) 267–294
- B5) (mit J. Beister) *Comprehensive Causal Specification of Asynchronous Circuit Behaviour: a Generalized STG.* Proc. 2nd Workshop Hardware Design and Petrinets (HWPN'99) within 20th International Conference on Application and Theory of Petri Nets, Williamsburg (Juni 1999) 149–168

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- B7) (mit W. Vogler) *Decomposition in Asynchronous Circuit Design*. In: M. Agrawal, A. Seth (Hrsg.): *FSTTCS 2002: Foundations of Software Technology and Theoretical Computer Science*. Lect. Notes Comp. Sci. 2556, Springer (2002) 336-347
- B8) M. Schaefer, W. Vogler, R. Wollowski, and V. Khomenko. *Strategies for Optimised STG Decomposition*. *Application of Concurrency to System Design (ACSD) 2006*, IEEE 2006, 123-132
- B9) M. Schaefer, W. Vogler, D. Wist, R. Wollowski: *Avoiding irreducible CSC conflicts by internal communication*. 8th *Application of Concurrency to System Design (ACSD)*, IEEE (2008), 3-12 (Best Paper Award)
- B10) M. Schaefer, W. Vogler, D. Wist, R. Wollowski: *Avoiding irreducible CSC conflicts by internal communication*. *Fundamenta Informaticae*, Volume 95, Number 1, IOS Press 2009, 1–29 (Langfassung von B9)
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- B11) M. Schaefer, D. Wist, R. Wollowski: *DESII – enabling decomposition-based synthesis of complex asynchronous controllers* (Tool Paper). *Application of Concurrency to System Design (ACSD) 2009*
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- B12) V. Khomenko, M. Schaefer, W. Vogler, R. Wollowski: *STG Decomposition Strategies in Combination with Unfolding*. *Acta Informatica*, Volume 46, Number 6, Springer (October 2009), 433-474
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- B13) D. Wist, M. Schaefer, W. Vogler, R. Wollowski: *STG Decomposition: Internal Communication for SI Implementability*. *ACSD'10: 10th Application of Concurrency to System Design*, IEEE 2010, 13 – 23
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- B14) D. Wist, W. Vogler, R. Wollowski: *STG Decomposition: Partitioning Heuristics*. *ACSD'11: 11th International Conference on Application of Concurrency to System Design*, 2011
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- B15) D. Wist, M. Schäfer, W. Vogler, R. Wollowski: *Signal Transition Graph Decomposition: Internal Communication for Speed Independent Implementability*. *IET Computers & Digital Techniques*, Volume 5, Issue 6, IEEE (2011), 440-451 (Zeitschriftenfassung von B13)

- B16) Norman Kluge, Ralf Wollowski: *Optimising Bundled-Data Balsa Circuits*. In Proceedings of the 2016 22nd IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC'16), pages 99-106, May 2016.

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- B17) Norman Kluge, Ralf Wollowski: *Data Path Optimisation and Delay Matching for Asynchronous Bundled-Data Balsa Circuits*. In Proceedings of the 2017 International Conference on Computer-Aided Design (ICCAD'17), pages 408-415, November 2017.

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- C2) (mit M. Raff) Bestimmung zeit- und energieoptimaler Prozesse in Transportsystemen unter Verwendung von Petrinetzen. Universität Kaiserslautern, Lehrstuhl für Digitaltechnik, Bericht B12-11.90 (1990)
- C3) (mit M. Raff) Modellierung und Analyse eines Container-Umschlagbahnhofs unter Verwendung von Petrinetzen. Beitrag zum GMD-Seminar Petri-Netze in der Praxis, Bonn (Dez. 1990)
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- C5) (mit B. Kangsah, W. Vogler, J. Beister) DESI: a Tool for Decomposing Signal Transition Graphs. Proc. 3rd ACiD-WG Workshop (organized by the Working Group on Asynchronous Circuit Design as part of the European Commission's Framework Programme FP5 Microelectronics), Crete, January 2003
- C6) (mit B. Kangsah, W. Vogler, J. Beister) DESI: a Tool for Decomposing Signal Transition Graphs. Tool Demonstration, Int. Conf. on Application of Concurrency to System Design ACSD 2005, Rennes, France (Juni 2005)

- C7) Dominic Wist, Ralf Wollowski. Avoiding Irreducible CSC Conflicts in Component STGs. Proceedings of the 19th UK Asynchronous Forum, Imperial College London, 2007 <http://cas.ee.ic.ac.uk/AsyncForum19/>
- C9) Dominic Wist, Ralf Wollowski. STG Decomposition: Avoiding Irreducible CSC Conflicts by Internal Communication. Technische Berichte des Hasso-Plattner-Instituts für Softwaresystemtechnik an der Universität Potsdam, Heft 20 (2007), ISBN 978-3-940793-02-7, ISSN 1613-5652
- C10) Mark Schaefer, Walter Vogler, Dominic Wist and Ralf Wollowski. Avoiding Irreducible CSC Conflicts by Internal Communication. Technical Report, Institute of Computer Science, University of Augsburg, February 2008
- C11) D. Wist, M. Schaefer, W. Vogler, R. Wollowski: STG Decomposition: Internal Communication for SI Implementability. Technische Berichte des Hasso-Plattner-Instituts, Heft 32 (2010), ISBN 978-3-86956-037-3, ISSN 1613-5652
- C12) N. Kluge, R. Wollowski: Completing the Resynthesis Flow for Balsa Circuits by Focusing on the Data Path – First Experiments. International Symposium on Asynchronous Circuits and Systems (ASYNC 2014), “Fresh Ideas Session 5”, 14.5.2014