# Fetch Me If You Can

## Evaluating CPU Cache Prefetching and Its Reliability on High Latency Memory

*Fabian Mahling*
*Marcel Weisgut*
*Tilmann Rabl*

*@DaMoN 2025*

HPI Hasso Plattner Institut
Digital Engineering · Universität Potsdam

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# Contributions

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1. Microbenchmarks identifying CPU prefetching characteristics

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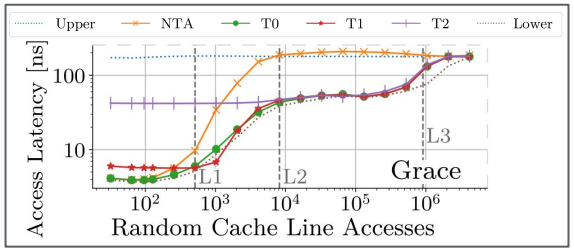


Localities

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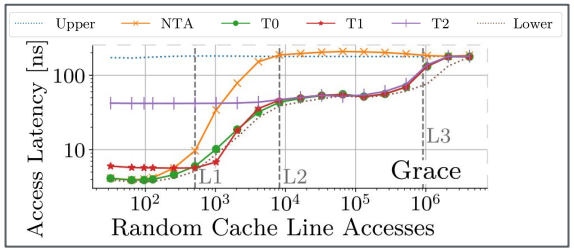


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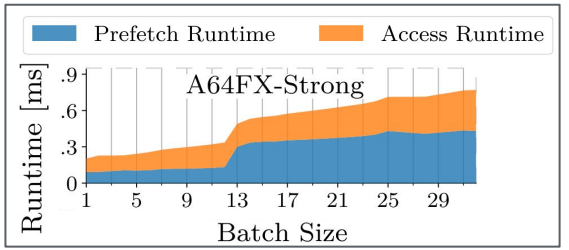


Reliability

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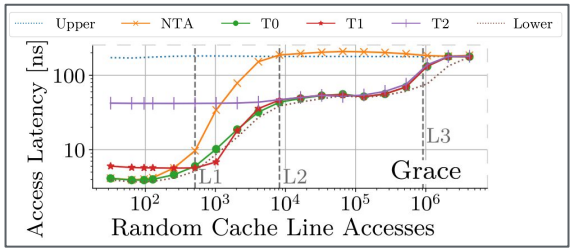


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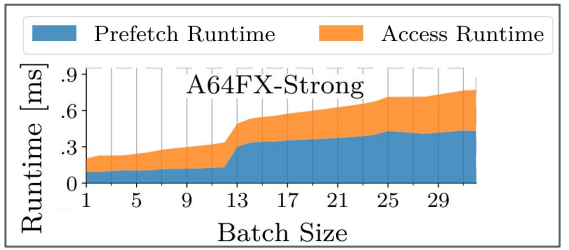


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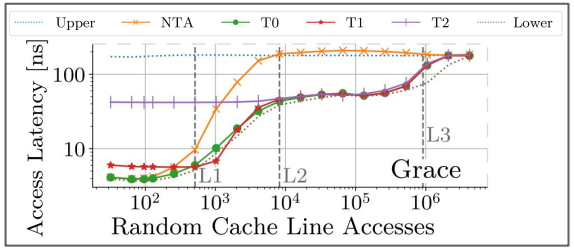


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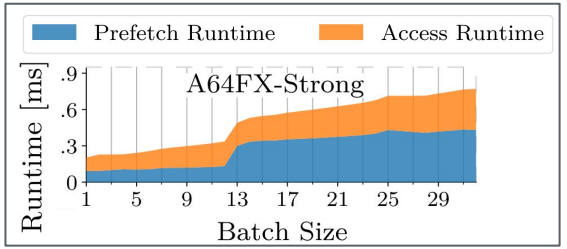


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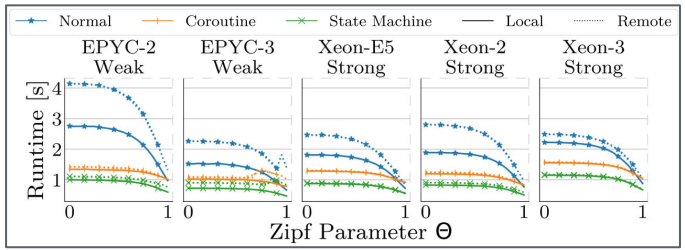


Binary Search

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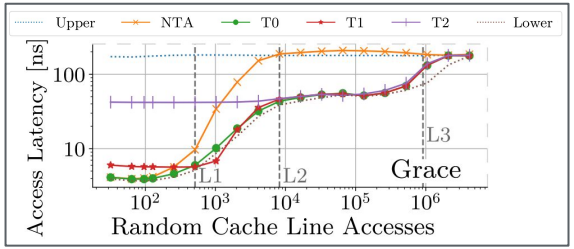


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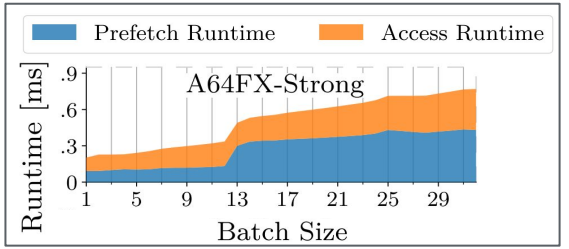


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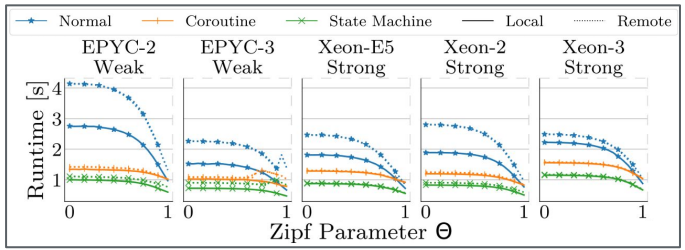


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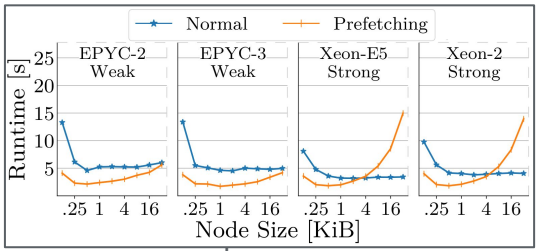


B$^+$-Tree

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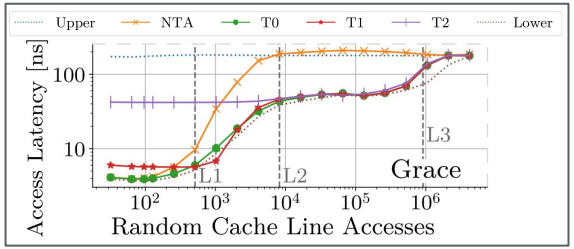


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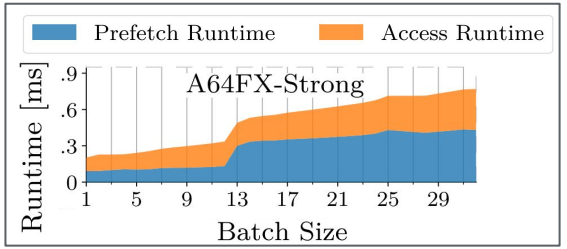


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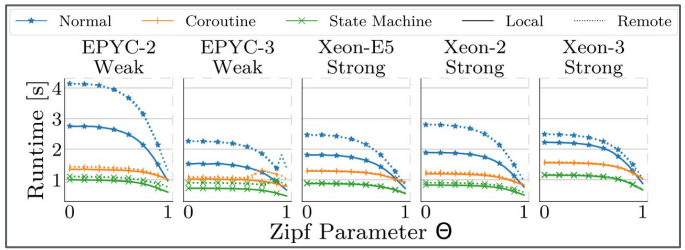


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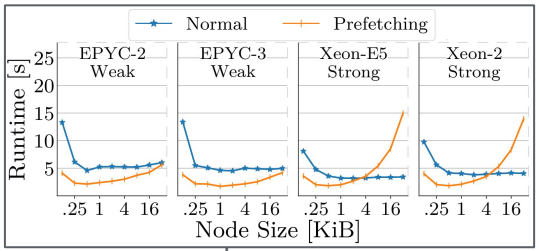


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3. Guidelines on when and how to use prefetching

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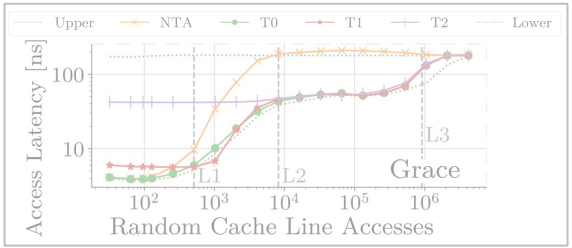


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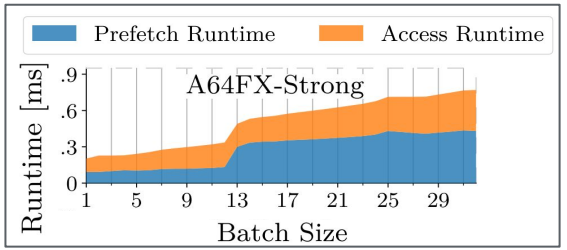


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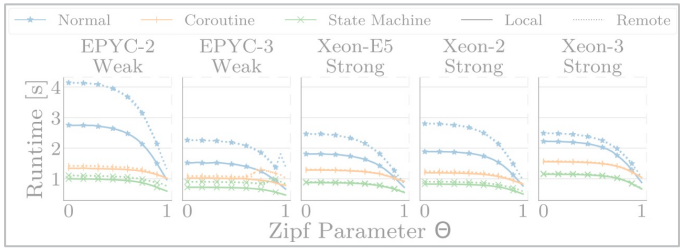


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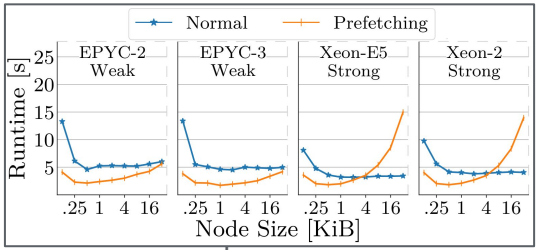


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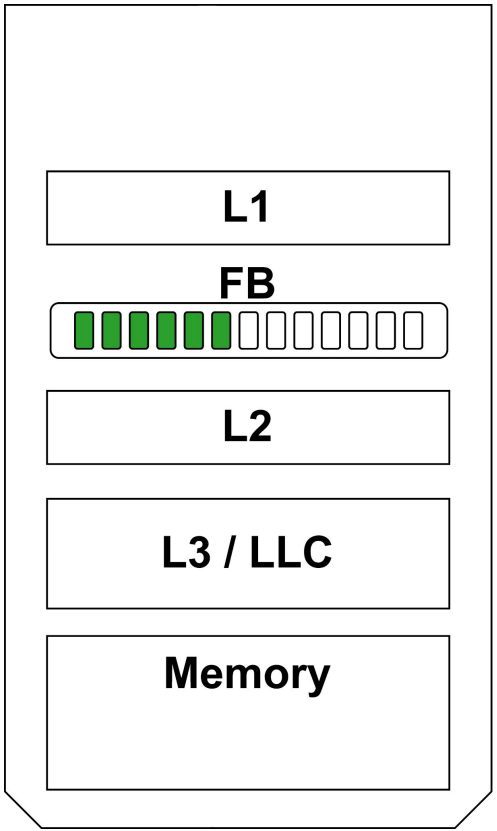
# Software Prefetching




Based on [*Kühn et al. 2024*]

- Asynchronous data movement to cache
- Locality specifies target cache level:

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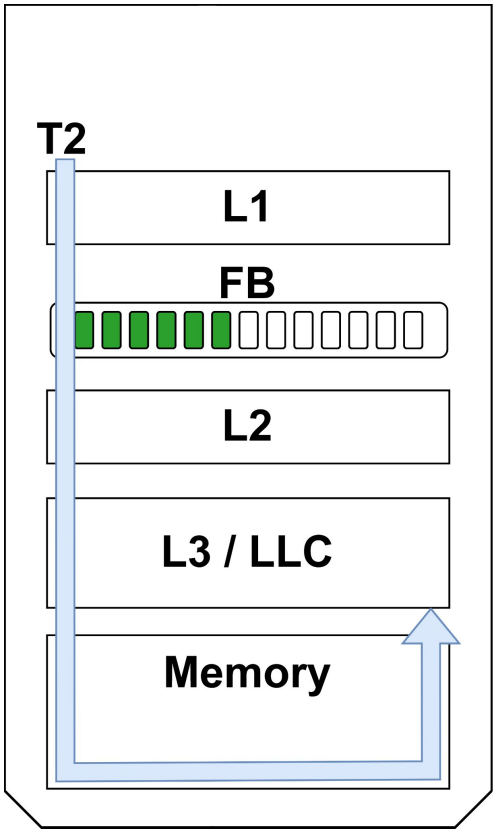


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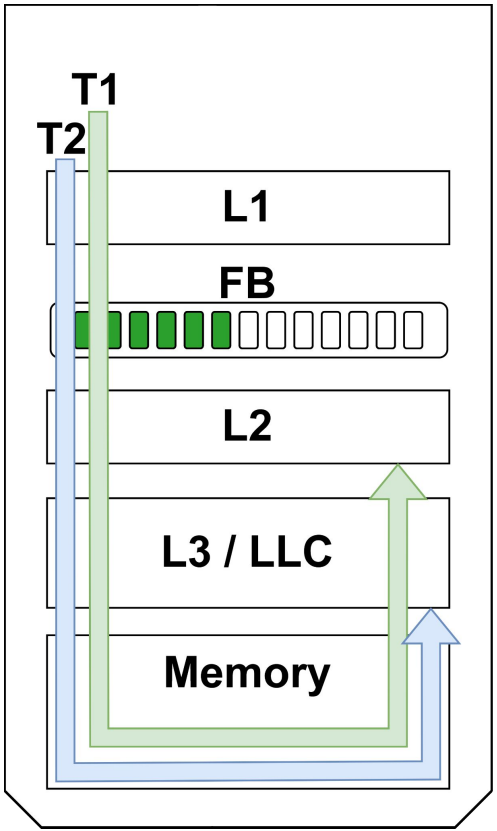


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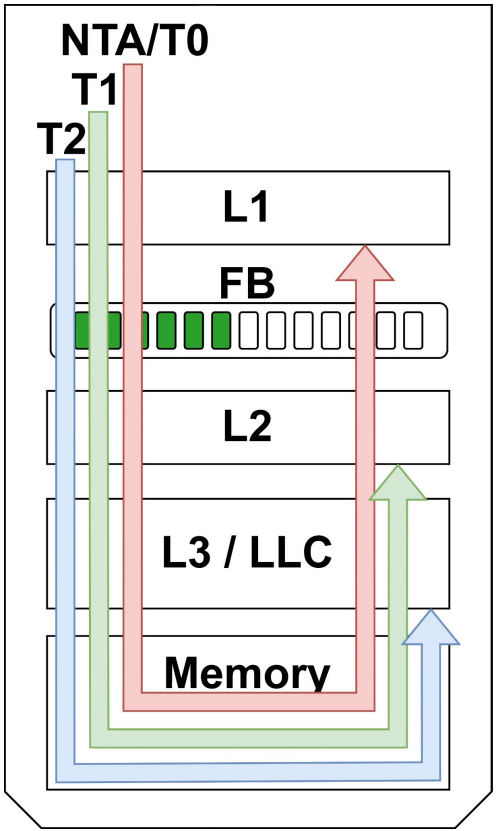


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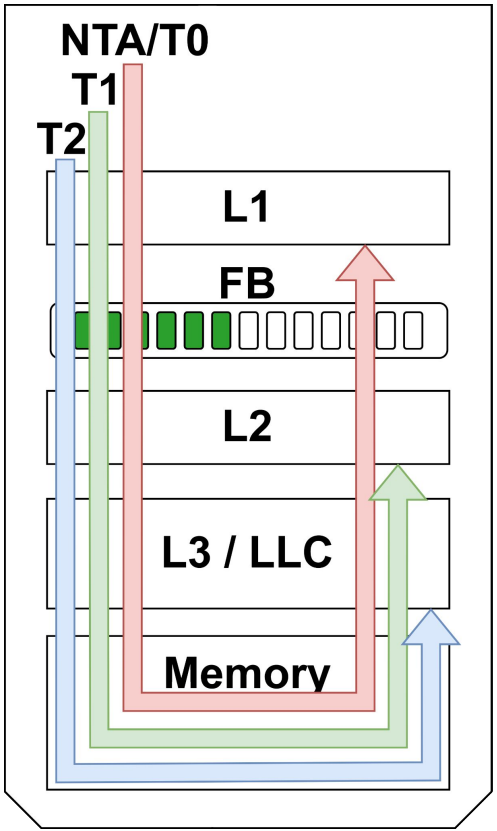


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- Locality specifies target cache level:
  - *T2* → *L3*
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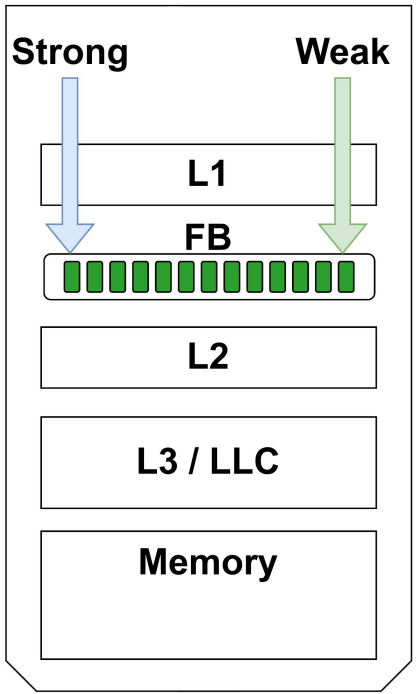
  - *T0 & NTA* → *L1*
- Hides memory access latencies through data movement ahead of the actual access

# Prefetching Reliability



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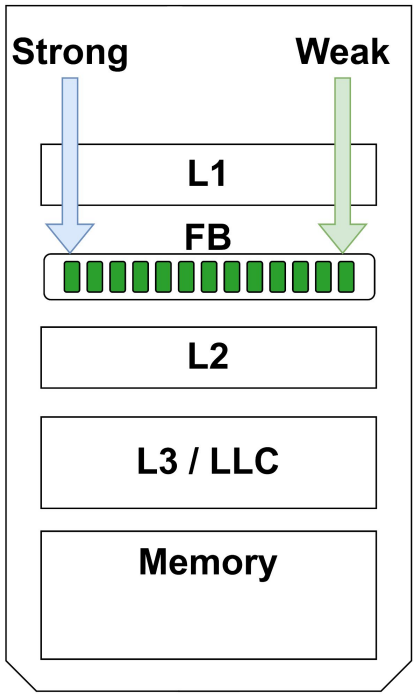
- **Strong** or **Weak** prefetching reliability



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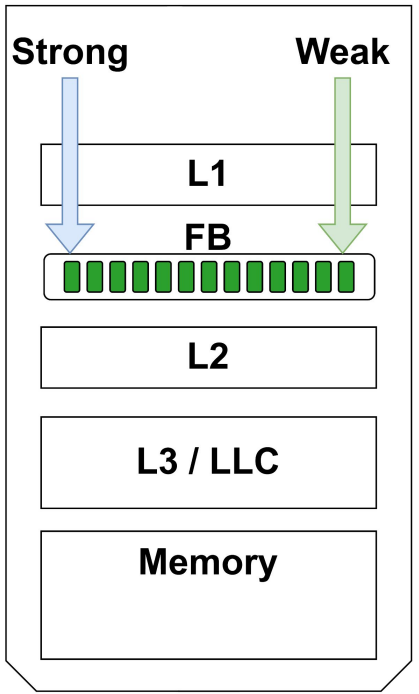

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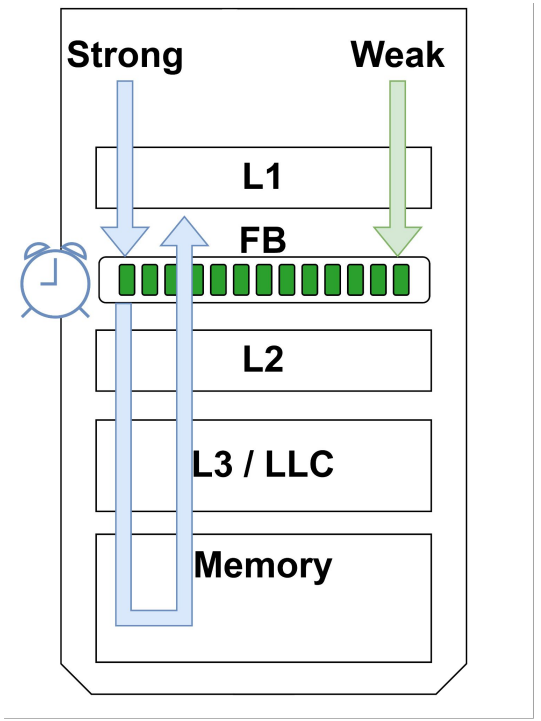

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- **Strong** or **Weak** prefetching reliability
- Different behavior for sparse hardware resources:
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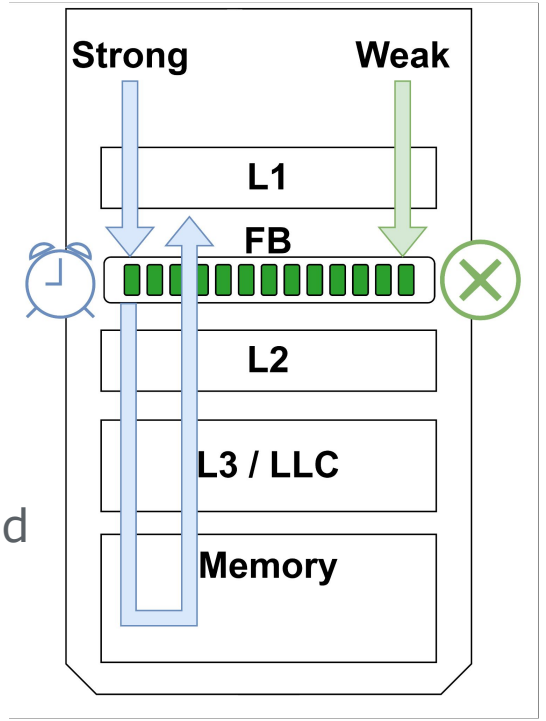
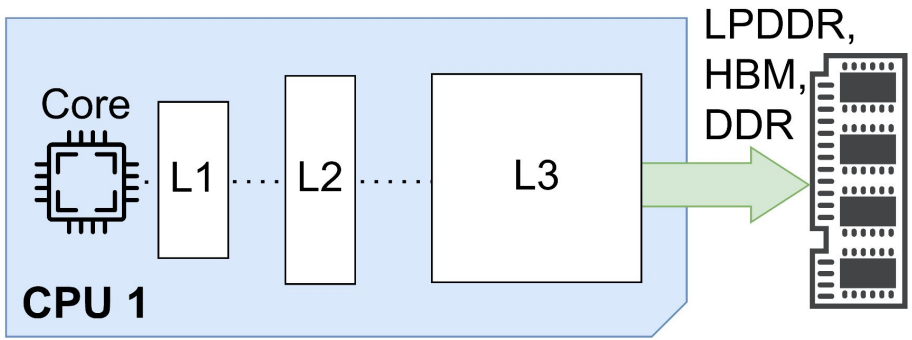
  - **Weak** *"Fetch Me, If You Can!":*
    - Drop prefetches when resources are occupied



# Used Systems

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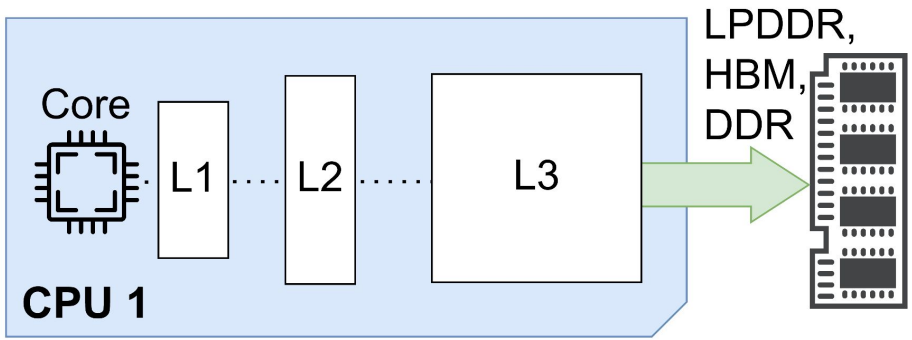


- Data Placement:

Based on [*Vuppalapati et al. 2024, Werner et al. 2025*]

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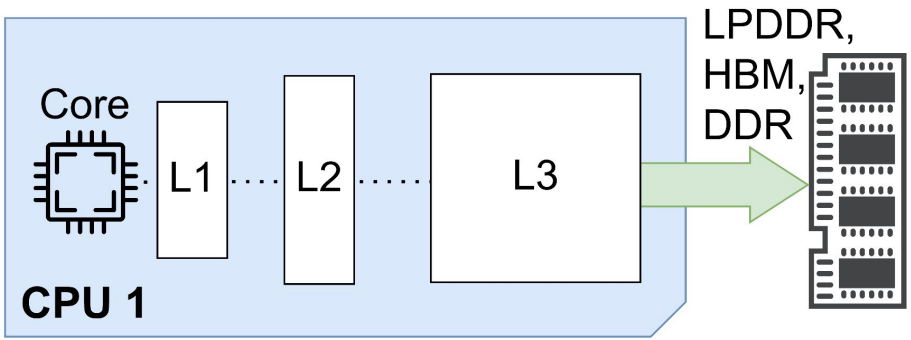


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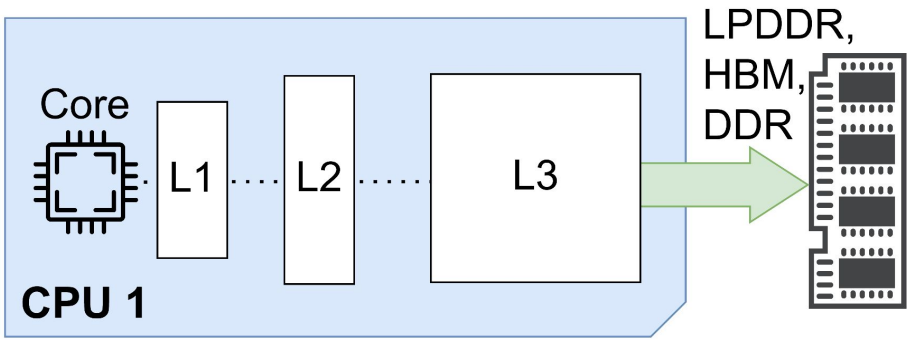


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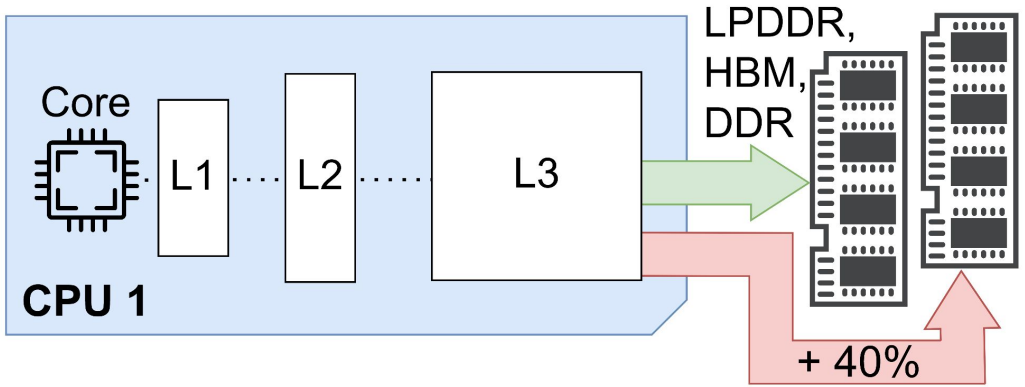


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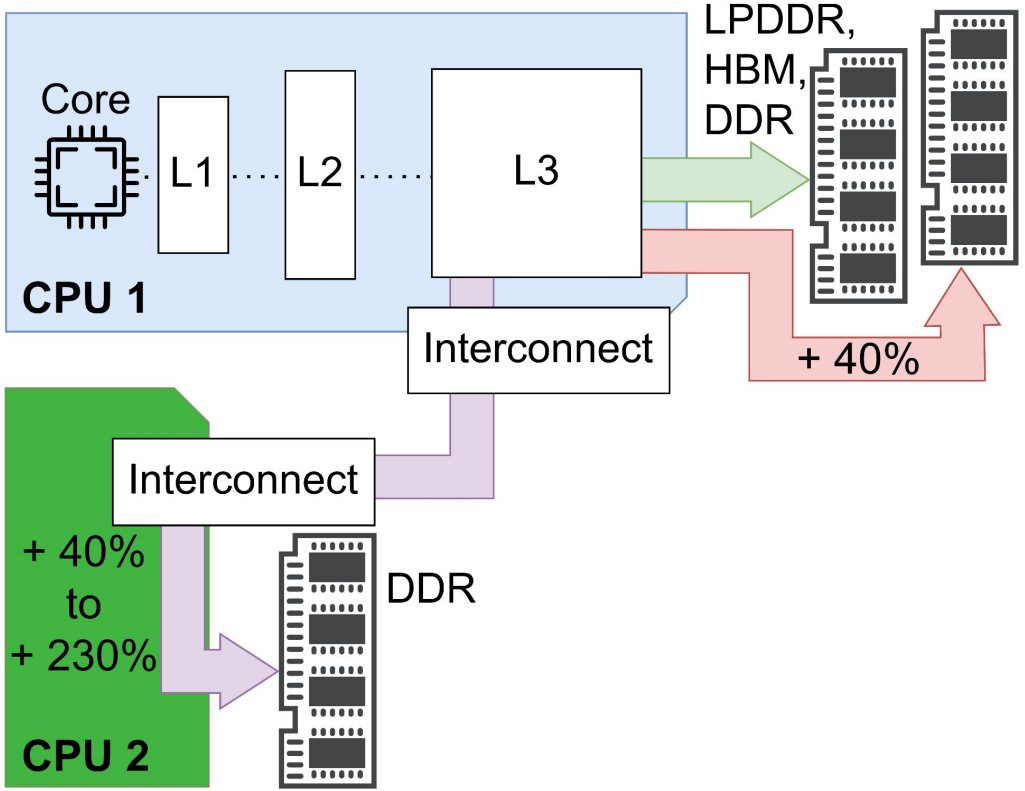


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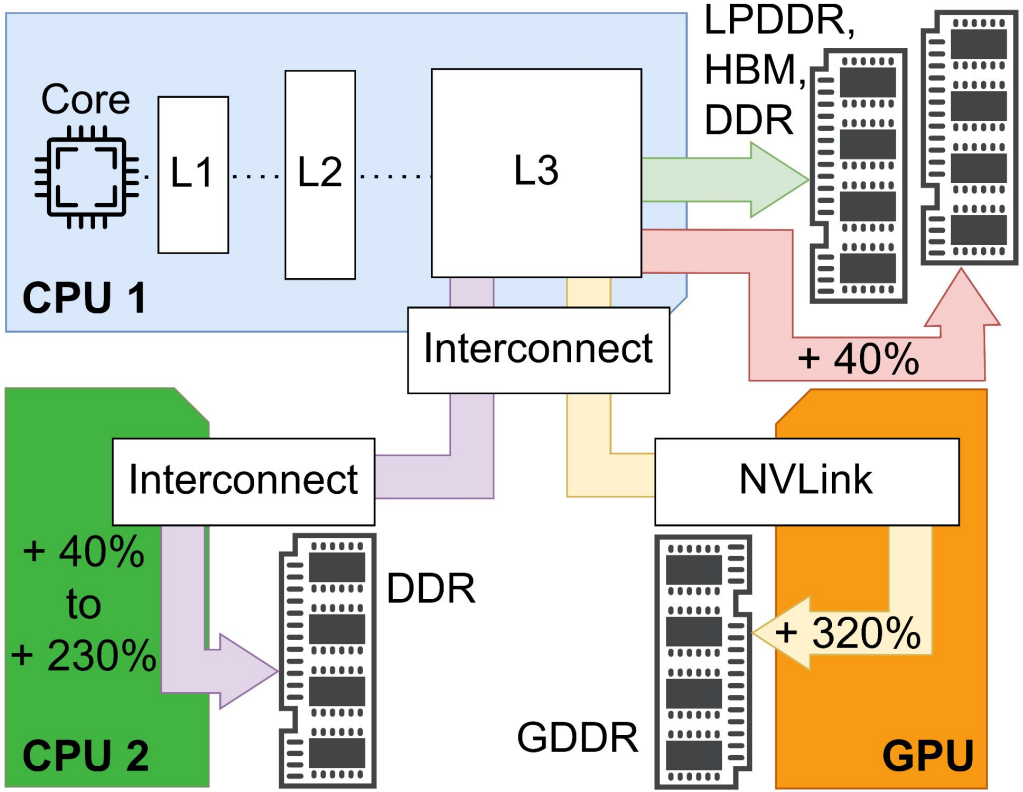


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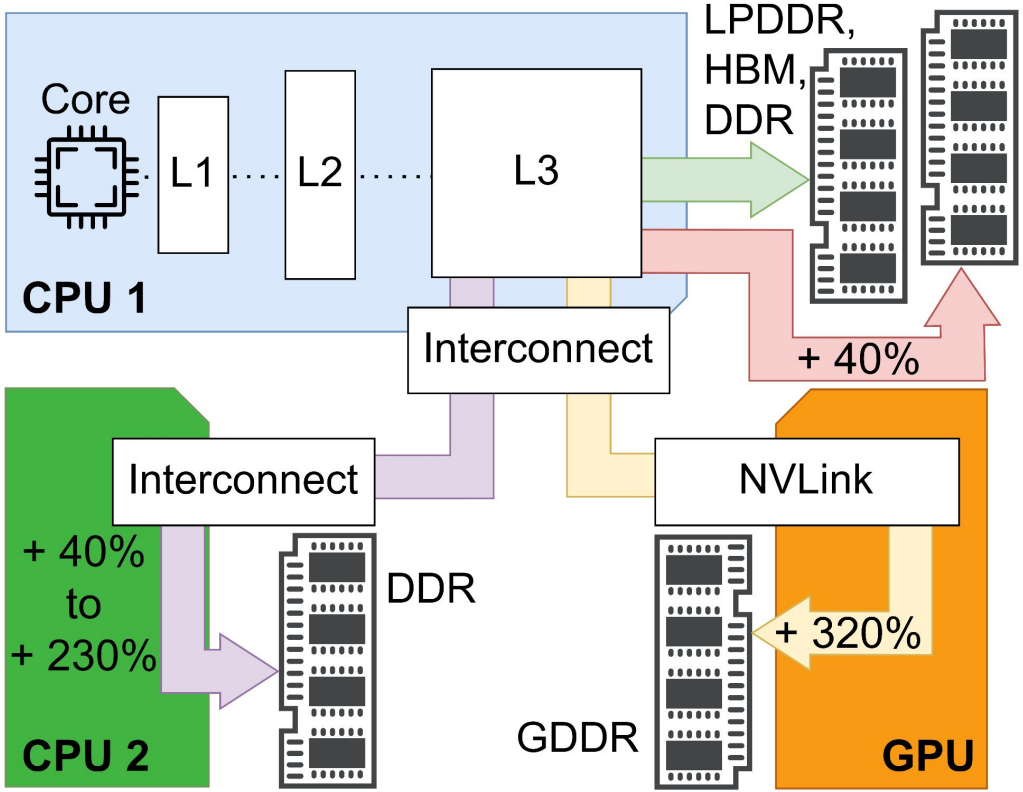


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- Different memory access paths have varying access latencies.

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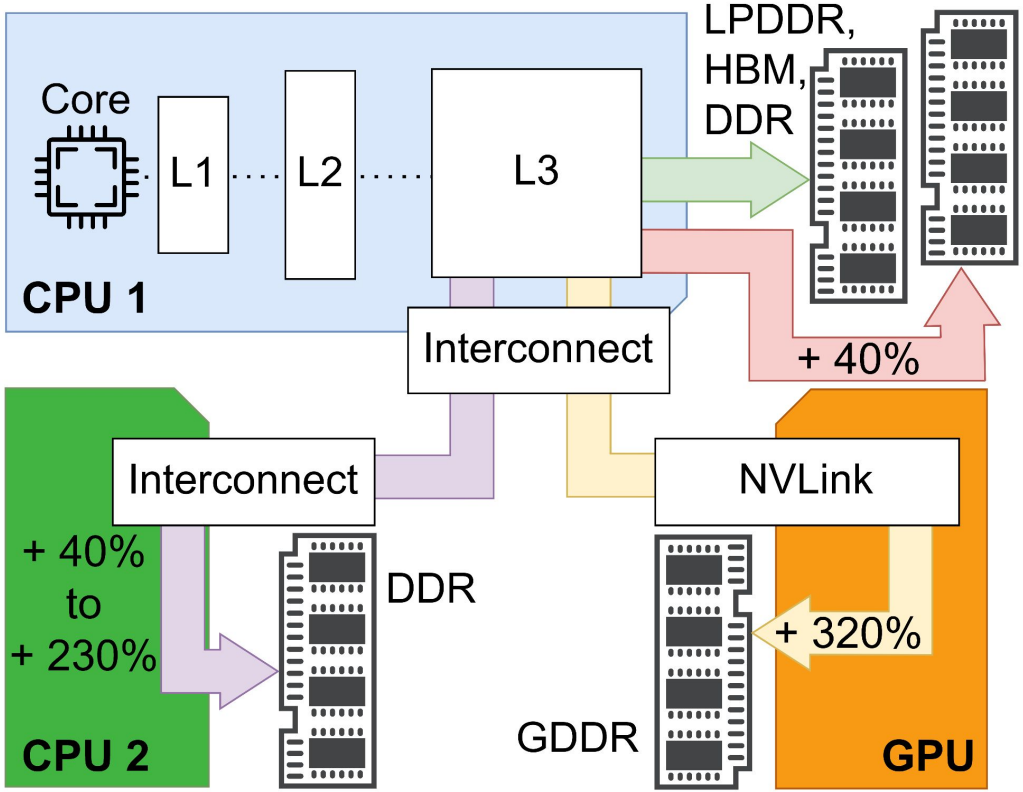


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- Data Placement:
  - **Local**: lowest latency
  - **Remote**: highest latency
- Different memory access paths have varying access latencies.
- Higher access latencies cause performance loss.

*Research Question*

**Can Software Prefetching hide increased memory access latencies, independently of the given prefetching reliability?**

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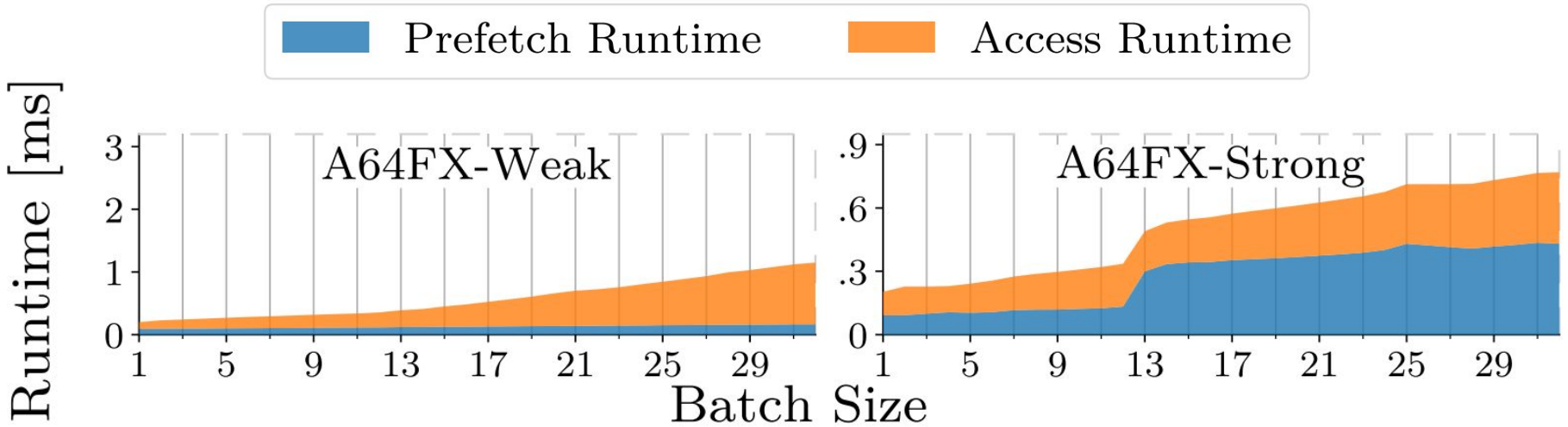

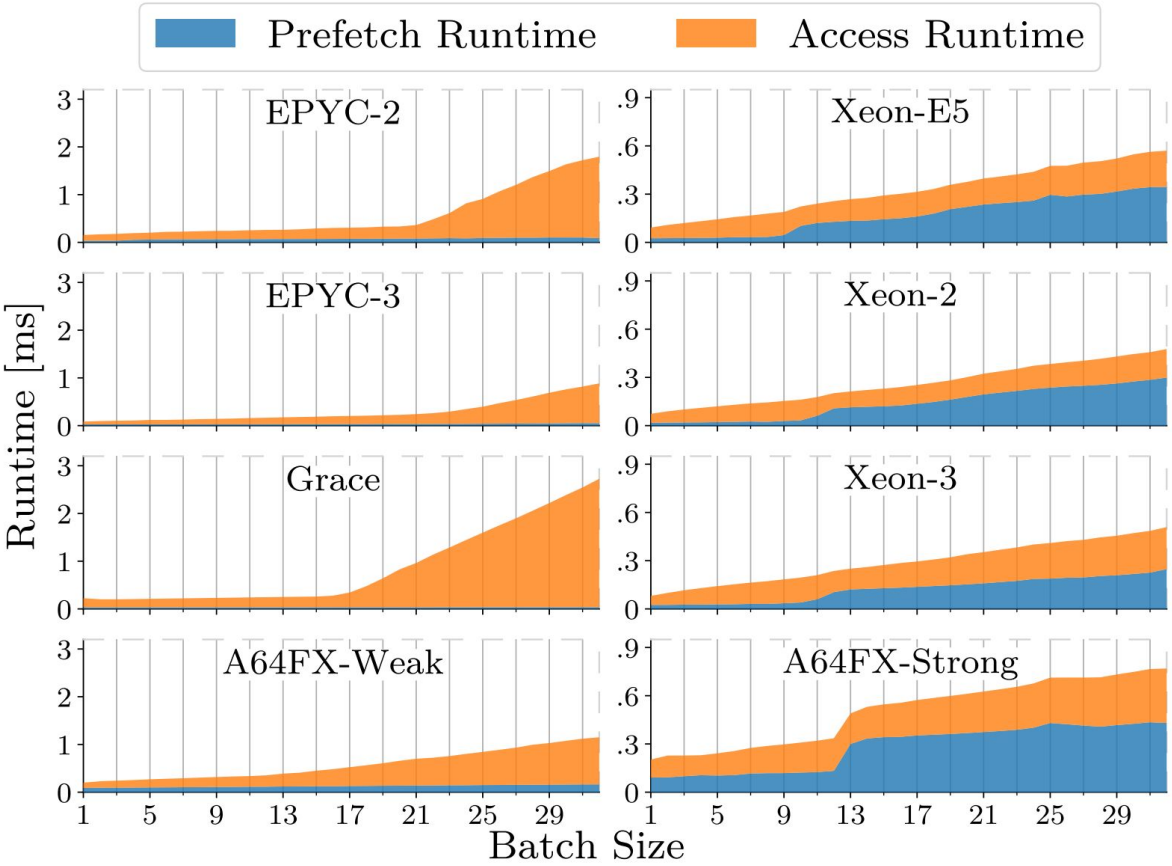
Prefetch Runtime
Access Runtime
EPYC-2
Xeon-E5
EPYC-3
Xeon-2
Grace
Xeon-3
A64FX-Weak
A64FX-Strong
Runtime [ms]
Batch Size
0
1
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3
.3
.6
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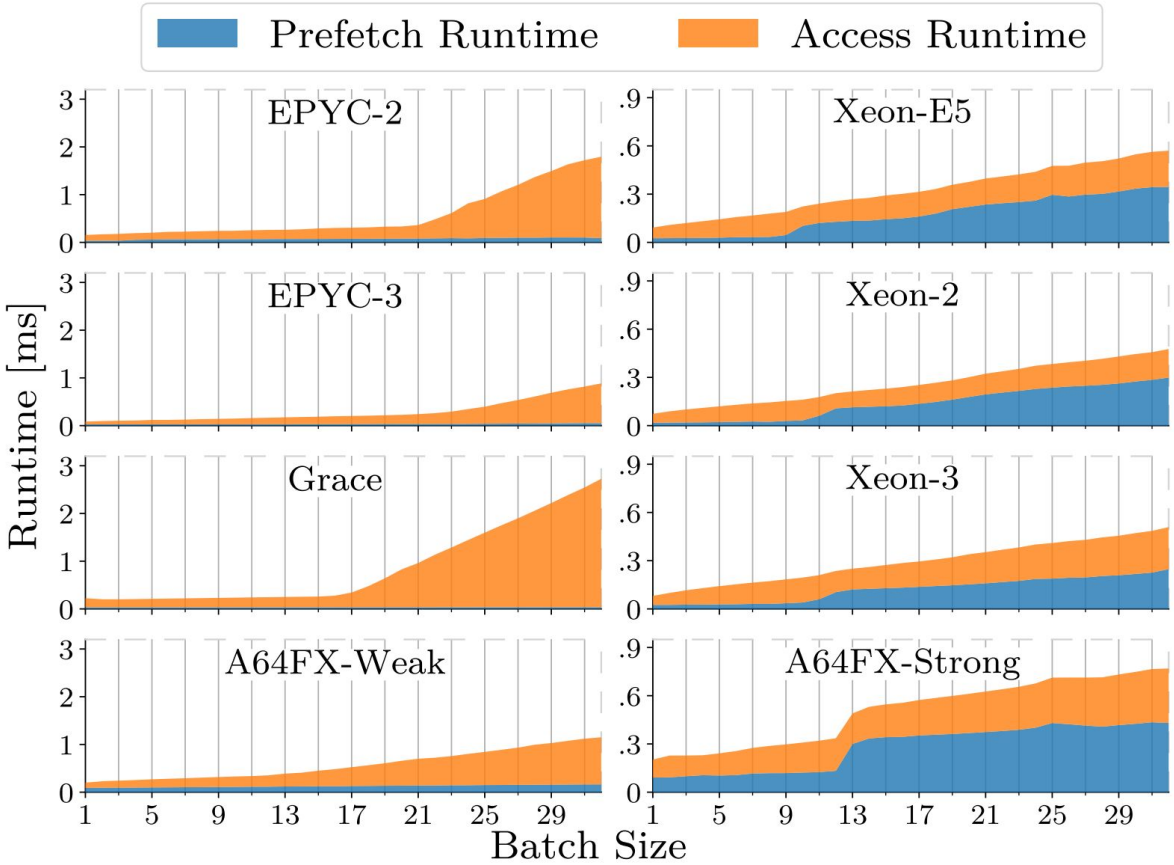


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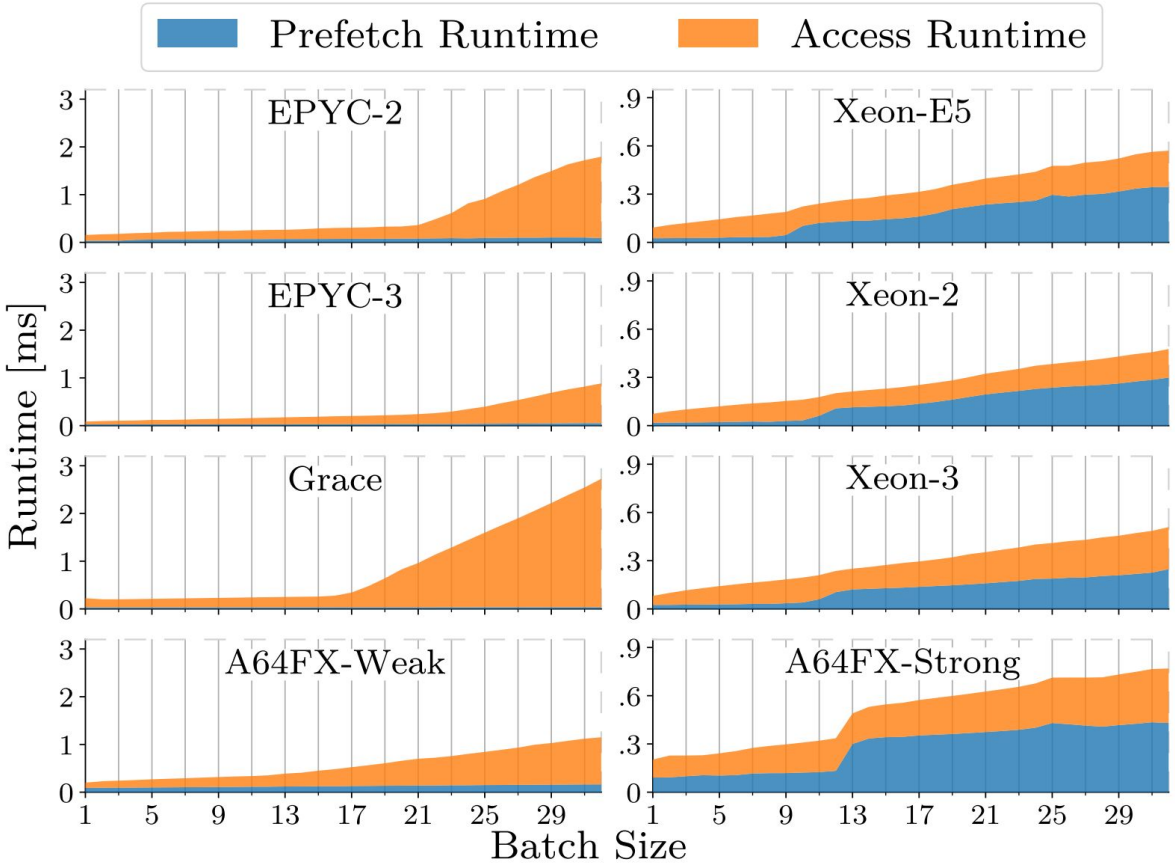


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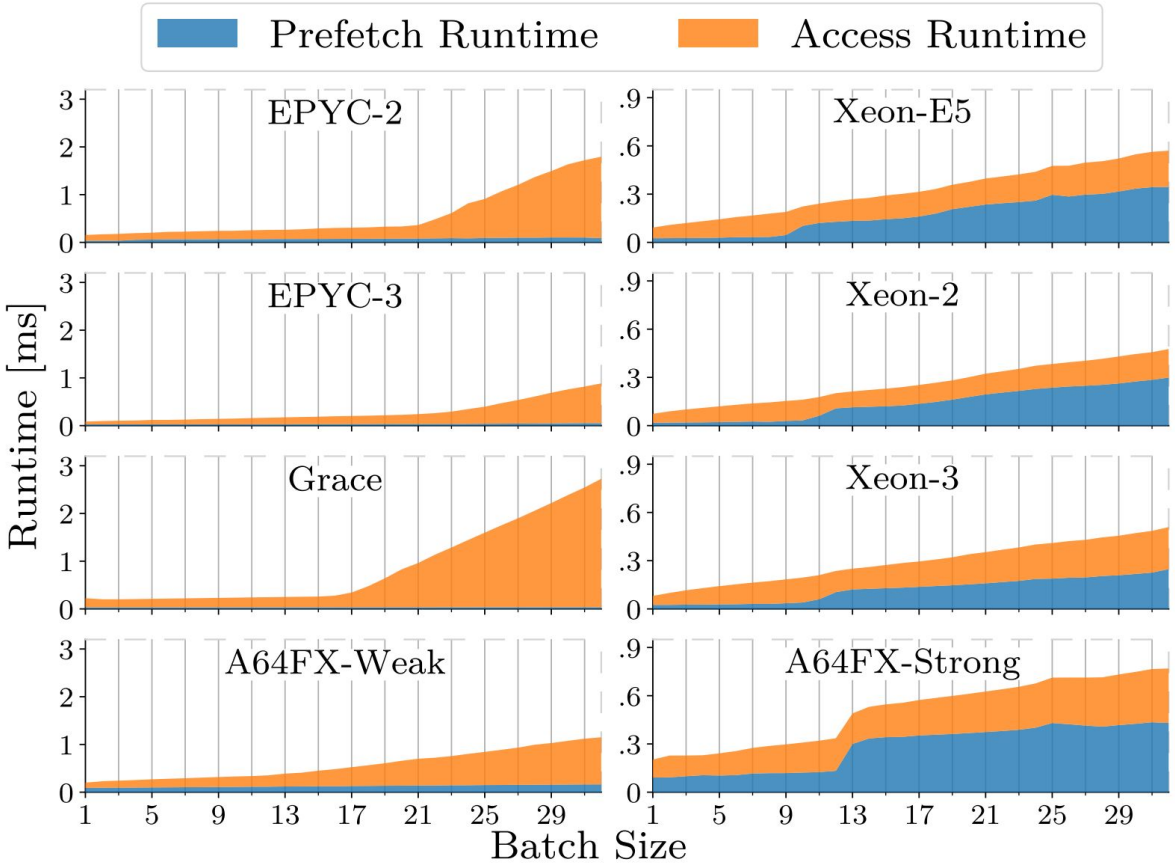
- Spike in (prefetching) runtime after a batch size of *X*

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- Spike in (prefetching) runtime after a batch size of *X*
  - *X* = FB size

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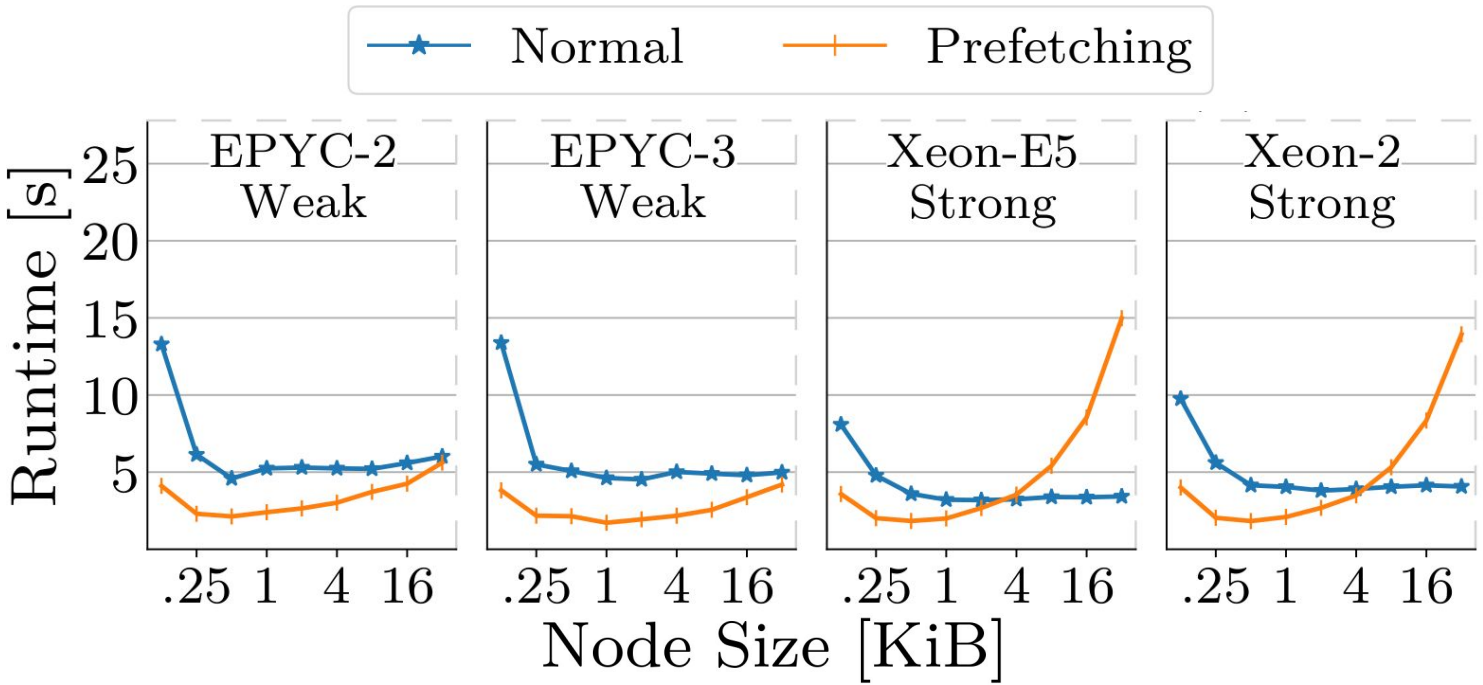

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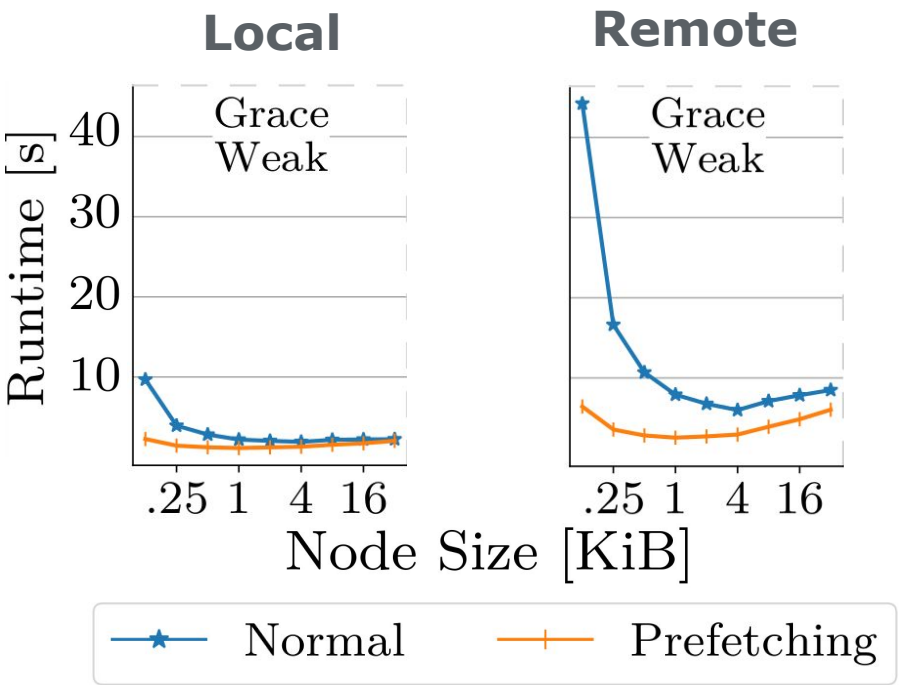

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- Prefetching can hide increased memory access latencies

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- Prefetching implementations vary across CPUs

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- Prefetching reliability important when prefetching speculatively
- Prefetching can hide increased memory access latencies

Future Work:

- Multithreaded experiments

# Conclusion & Future Work

Conclusion:

- Prefetching implementations vary across CPUs
  (prefetching reliability, target cache, eviction behavior)
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Future Work:

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Paper

Code

# Backup-Slides

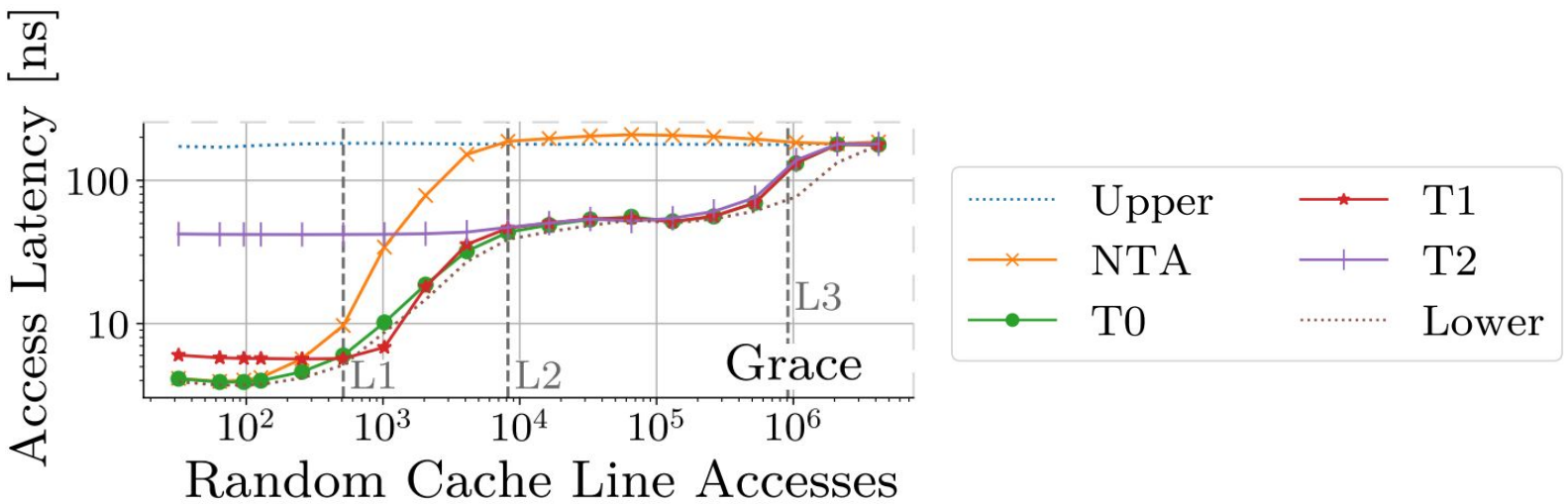
# High Latency Memory

- Heterogeneous memory causes varying access latencies
- 1.4x – 4.2x for used Systems
- **Problem:** Performance loss in latency bound workloads

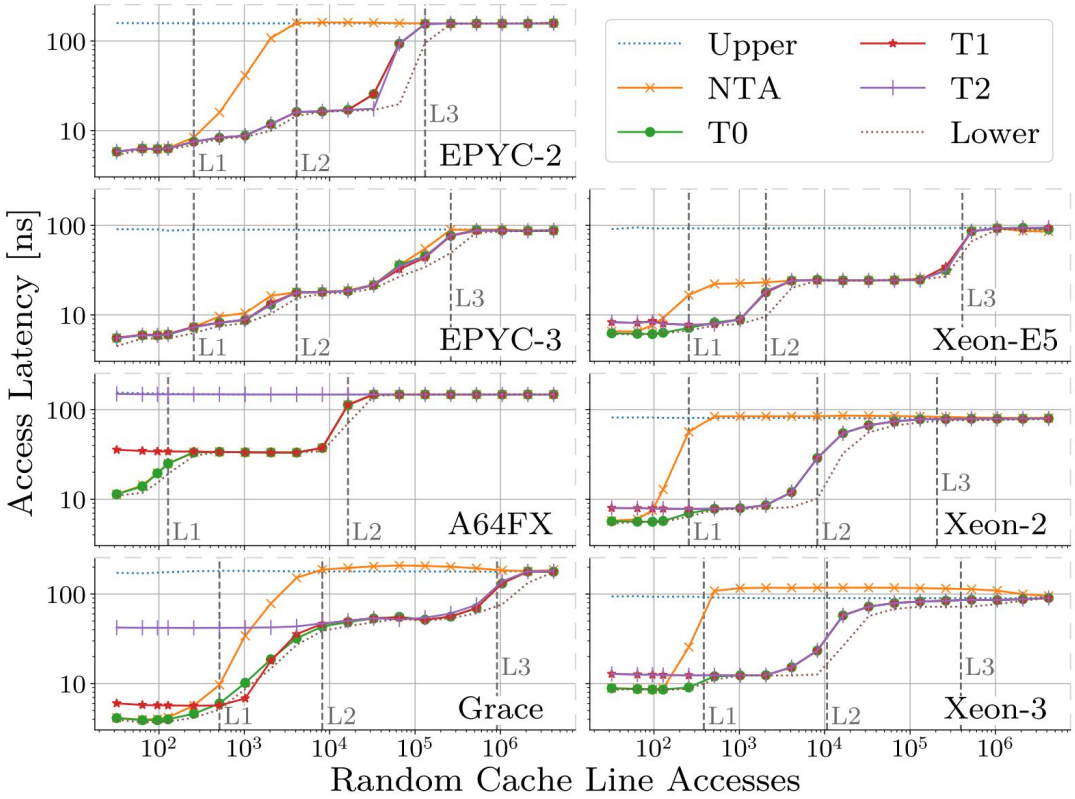
| ID | CPUs | Memory | Latency [ns] | |
|---|---|---|---|---|
| | | | Local | Remote |
| EPYC-2 | 2× 7742 | DDR4 | 153 | 277 |
| EPYC-3 | 2× 7413 | DDR4 | 83 | 272 |
| Xeon-E5 | 2× E5-2689 v4 | DDR4 | 80 | 130 |
| Xeon-2 | 2× 5220S | DDR4 | 76 | 156 |
| Xeon-3 | 2× 8352Y | DDR4 | 83 | 134 |
| A64FX | 1× A64FX | HBM2 | 215 | 307 |
| Grace | 1× Grace CPU | LPDDR5X HBM3 | 181 | 760 |

# CPU Prefetching Localities

- Prefetch batches of random cache lines with different localities
- Measure subsequent access latency
- Compare to accessed cache lines (Lower) and random cache lines (Upper)

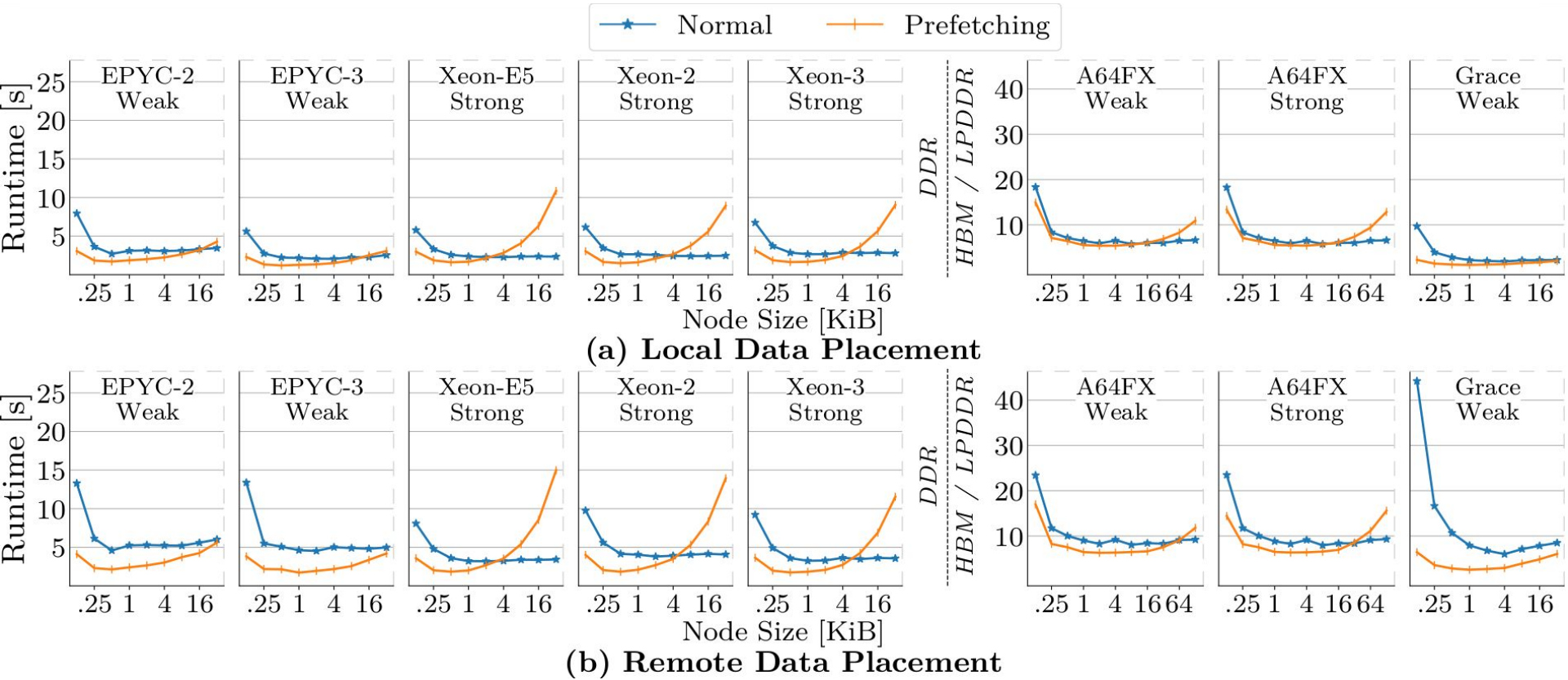


# CPU Prefetching Localities




- *T0* and *NTA* implementations consistent on most CPUs
- Other localities have varying implementations, even for the same CPU manufacturer

# CPU Prefetching Reliability - B$^+$-Tree



# CPU Prefetching High Latency - Binary Search

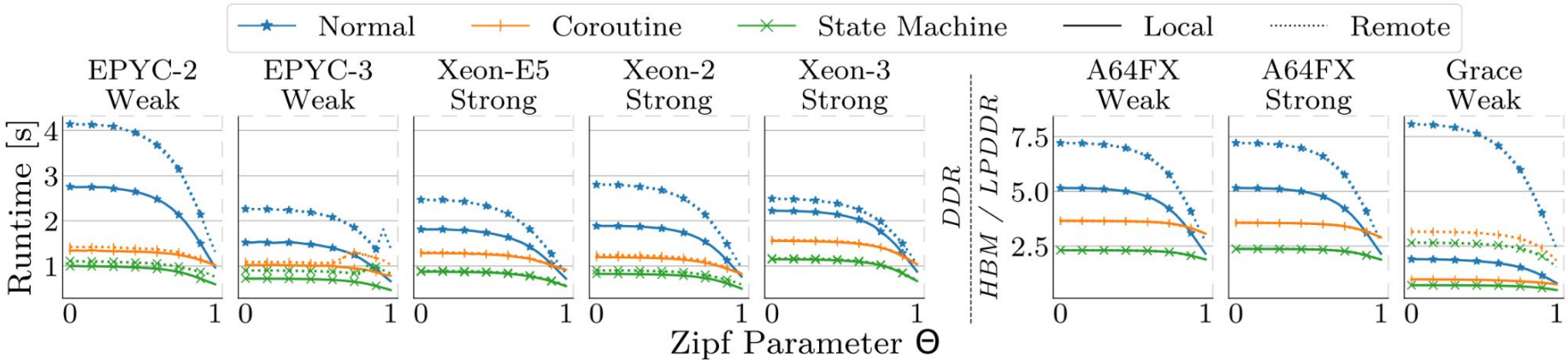



**Figure 6: Binary search runtimes given different data placement, implementations, and Zipf parameters.**