Research Track – Data Management on Novel Hardware

CXL Memory Performance for In-Memory Data Processing

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Technische Universität Munich, Munich, Germany

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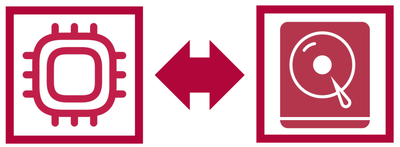
Hasso Plattner Institute, University of Potsdam, Potsdam, Germany

Resource Disaggregation



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Widely adopted.

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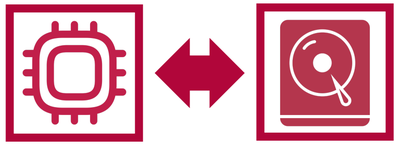

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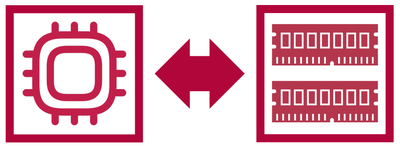

Increasing efforts on memory-disaggregated database systems [2, 3].

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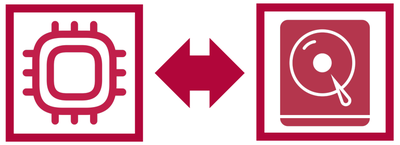

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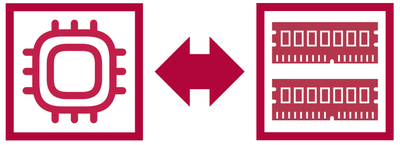

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CXL

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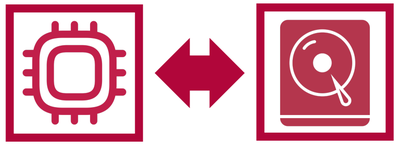

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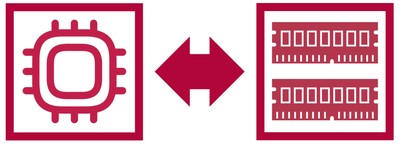

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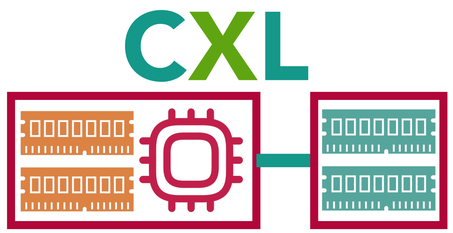

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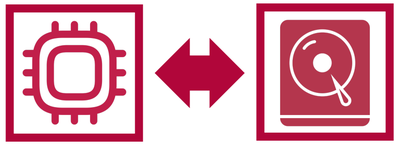

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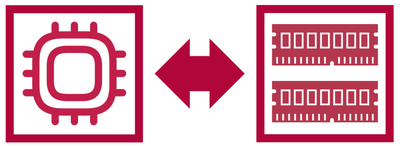

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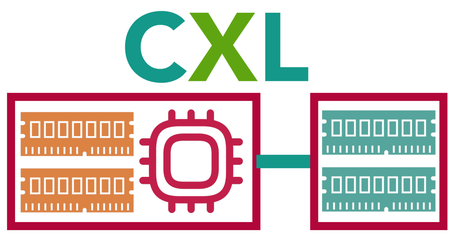

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Extensive experimentation required to identify what part of a database engine can be stored in CXL memory and what part should reside in CPU memory [2].

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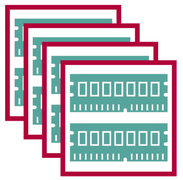

Memory access performance evaluation on a server with four CXL memory devices.

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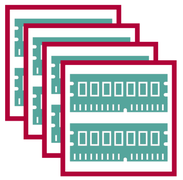

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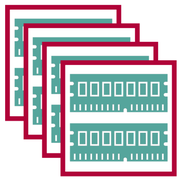

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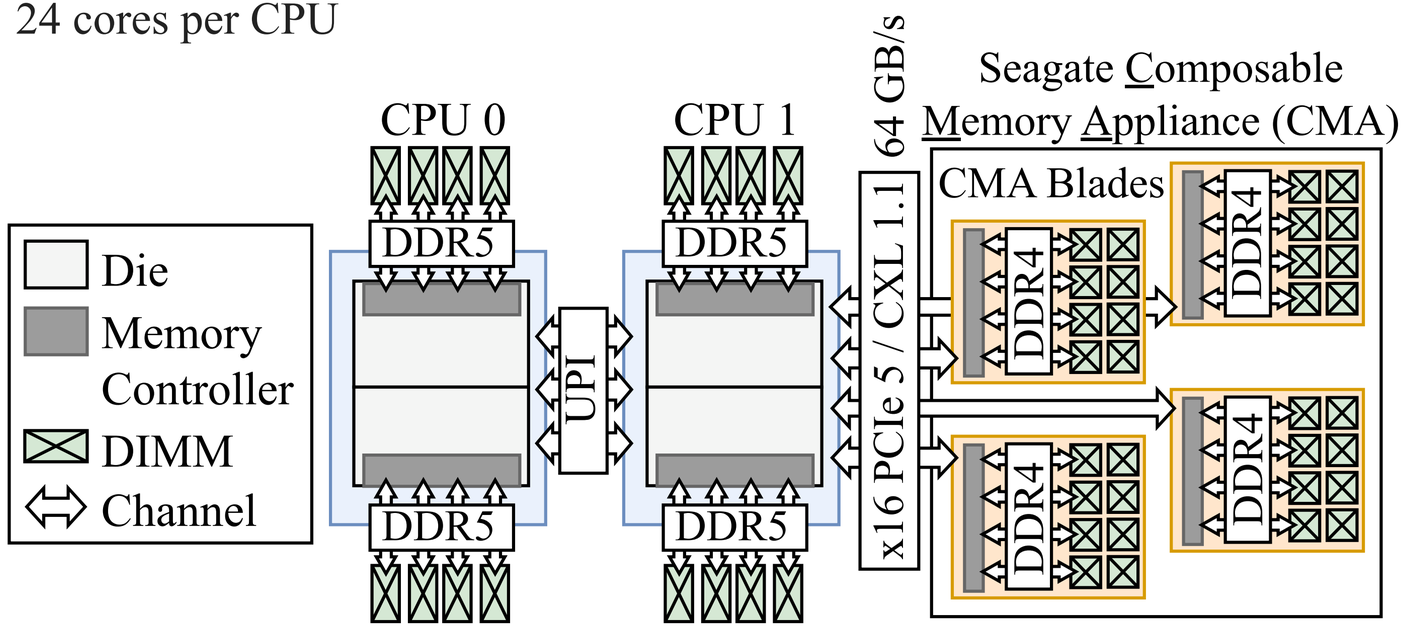
Hardware Setup

2× Intel Xeon Gold 6542Y (Emerald Rapids)
24 cores per CPU



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8 x 32 GiB DDR5 (4800 MT/s)

Memory per CMA blade:
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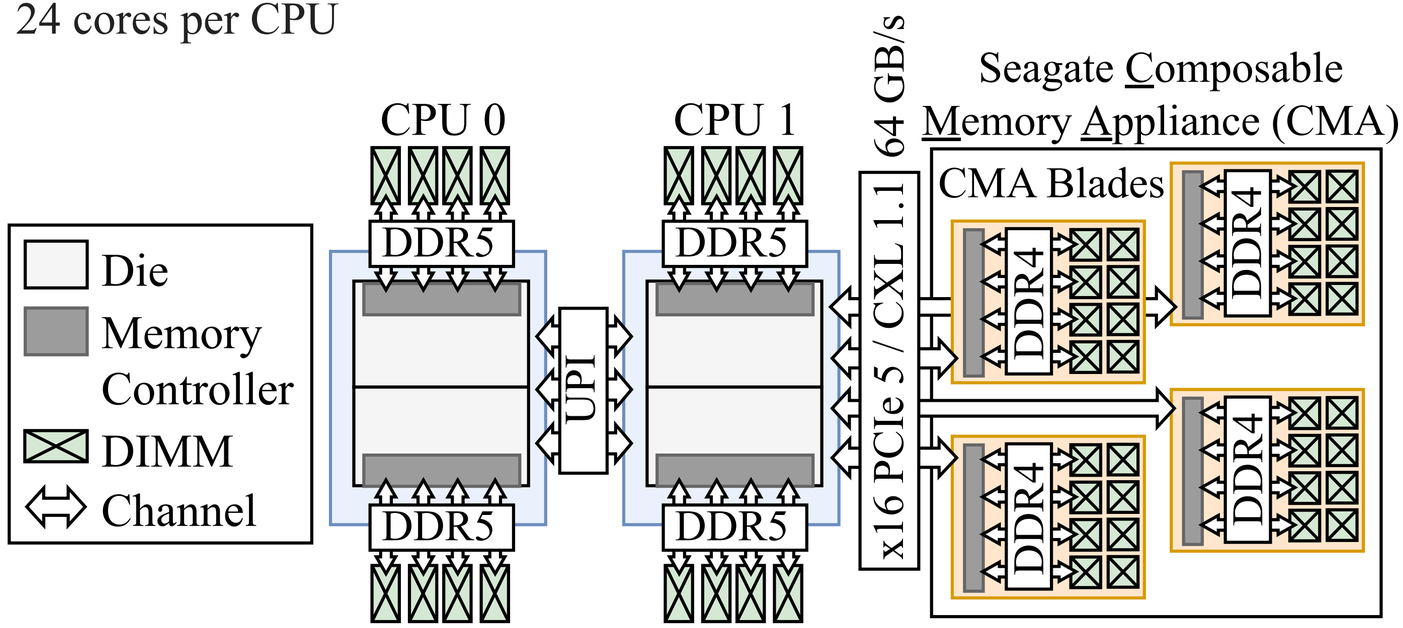

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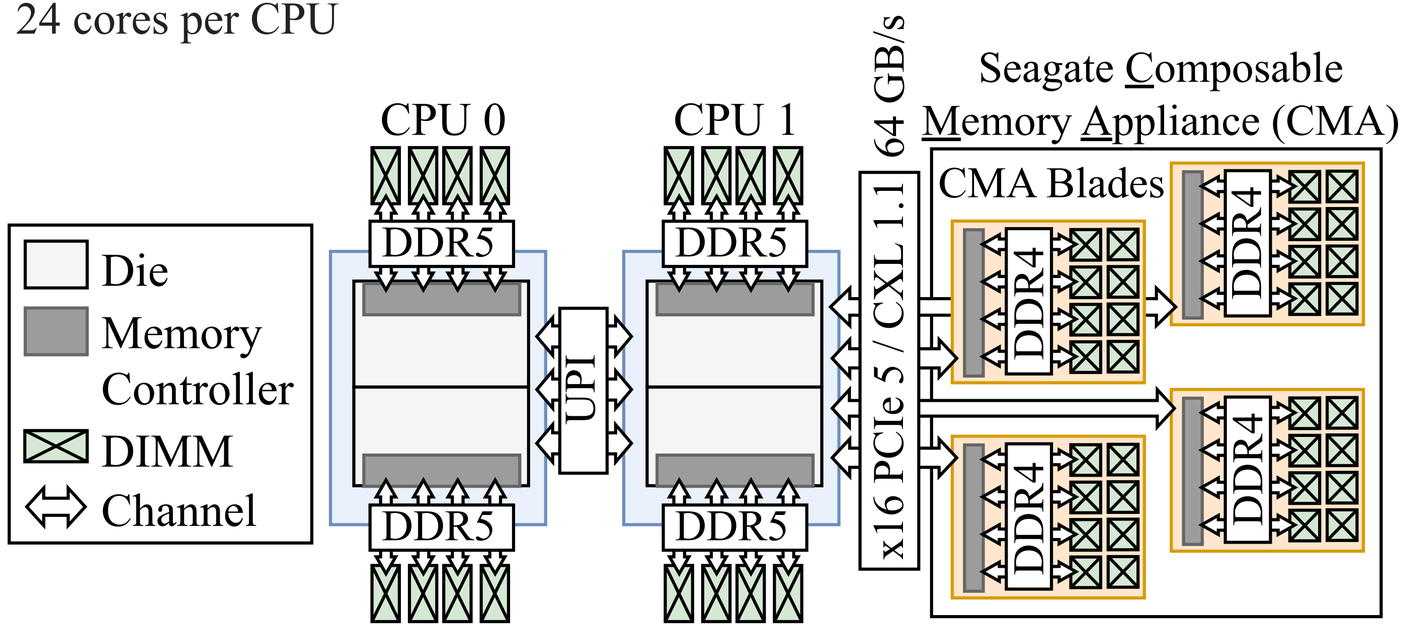

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Impact of storing table data in CXL memory ?

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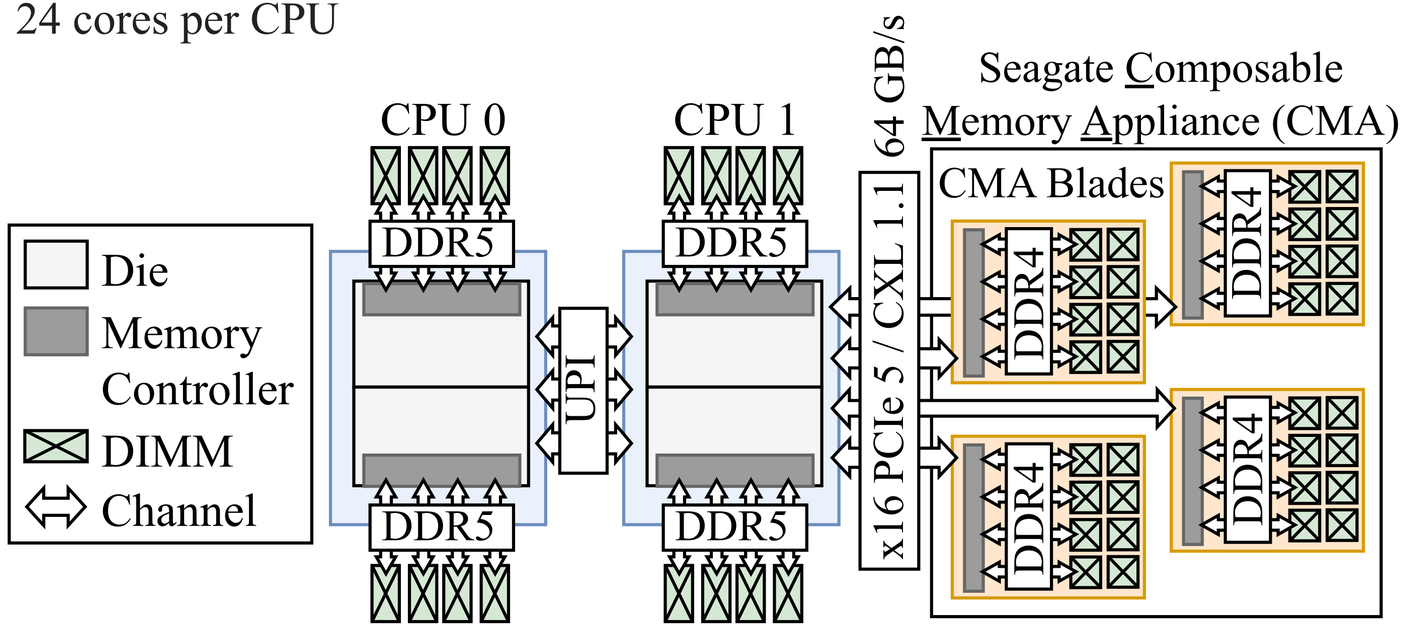

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HYRISE [5]

[5] Dreseler et al., Hyrise Re-engineered: An Extensible Database System for Research in Relational In-Memory Data Management, EDBT.

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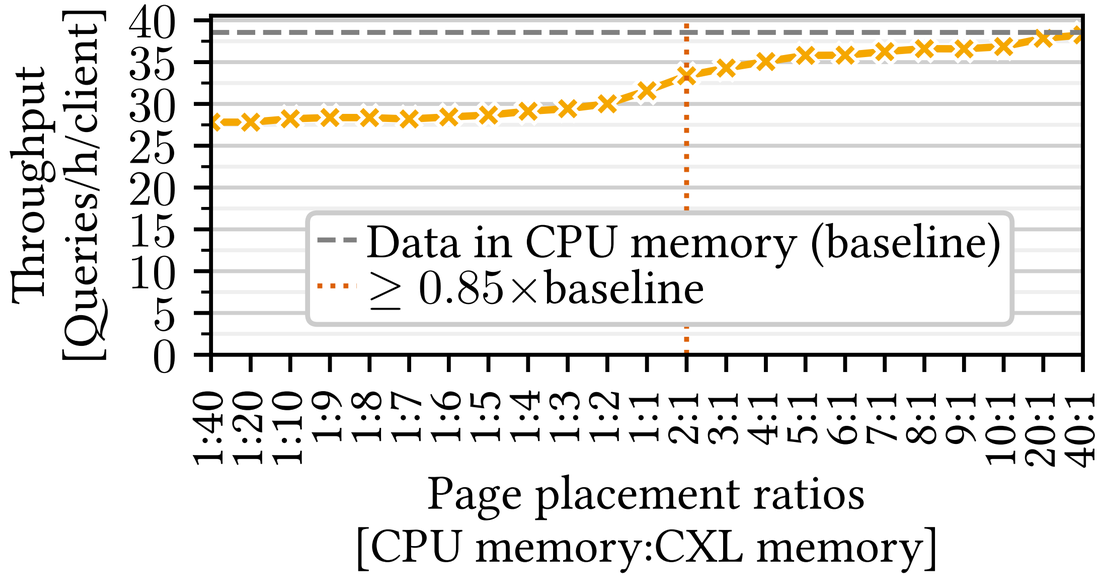
Black Box Approach (Page Granularity)



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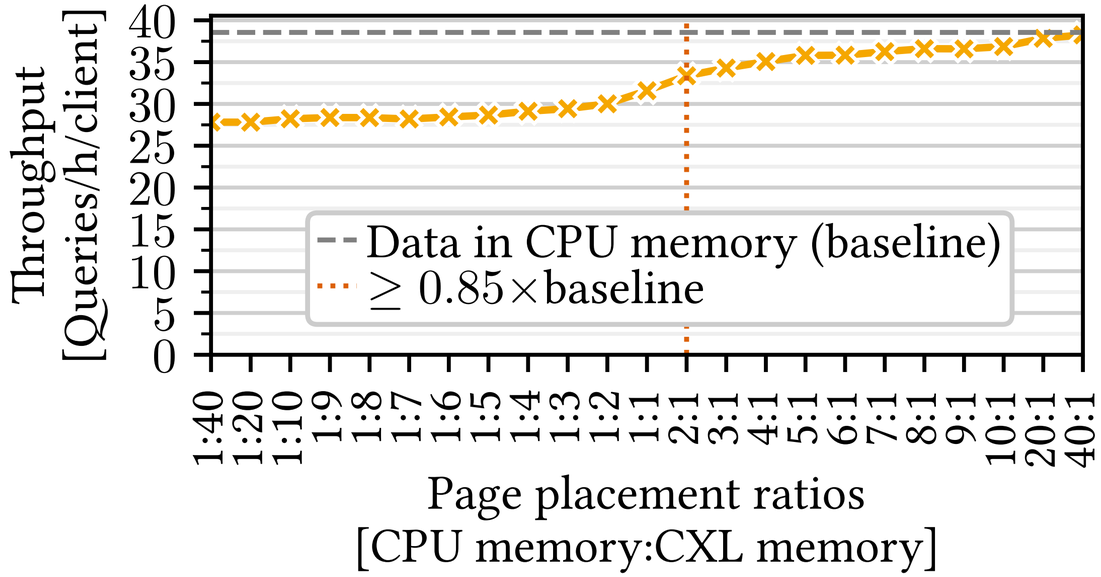

- Data placement via page interleaving across CPU memory and one CXL device

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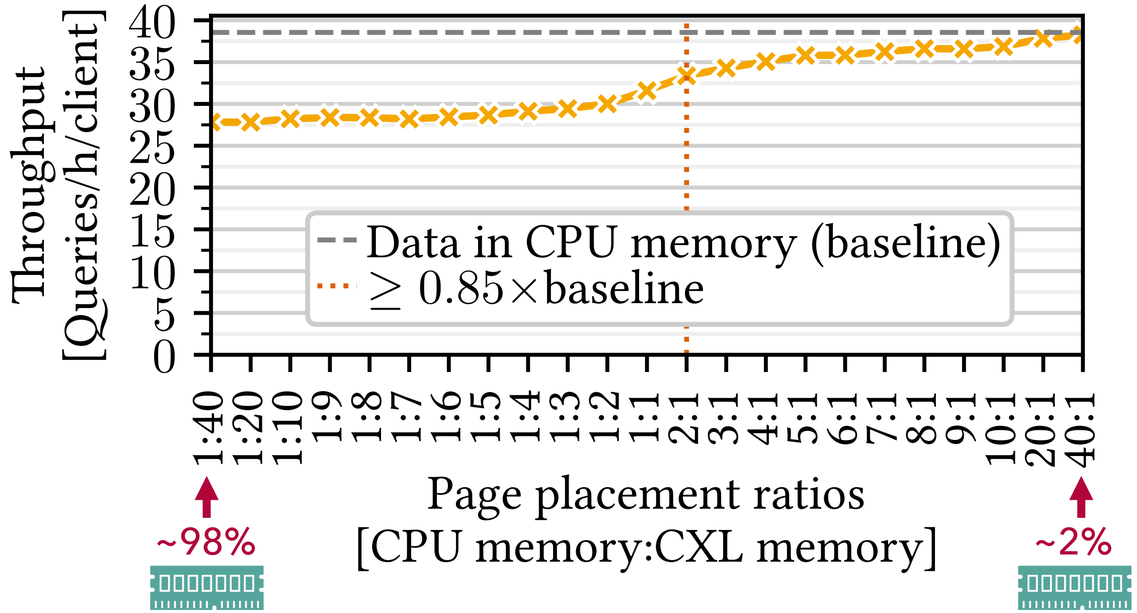

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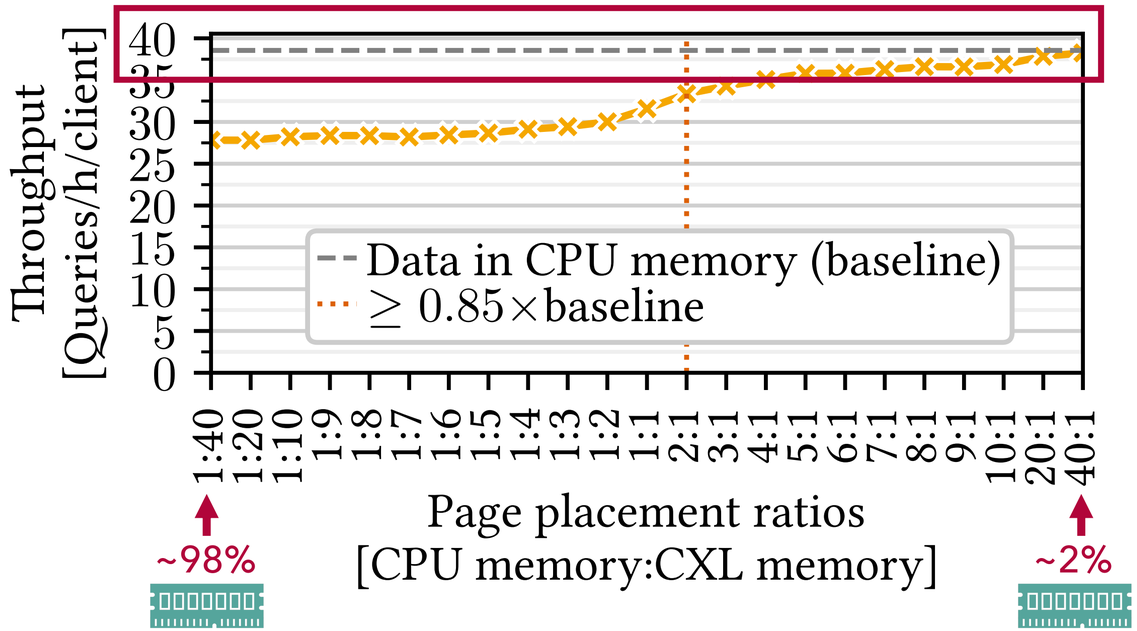

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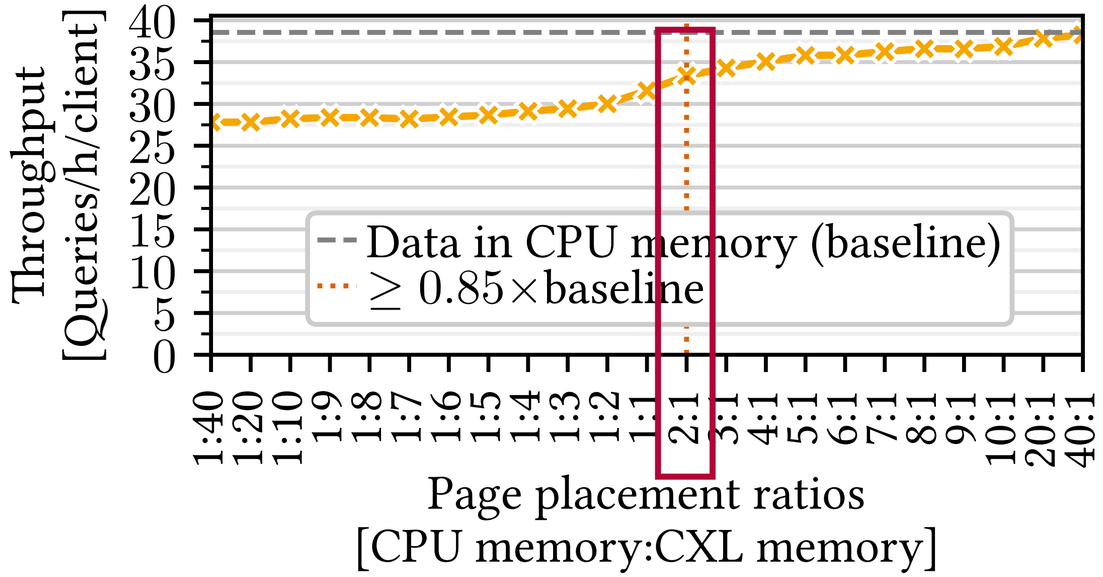

- Data placement via page interleaving across CPU memory and one CXL device
- 2:1 stores only $\frac{1}{3}$ pages in CXL memory

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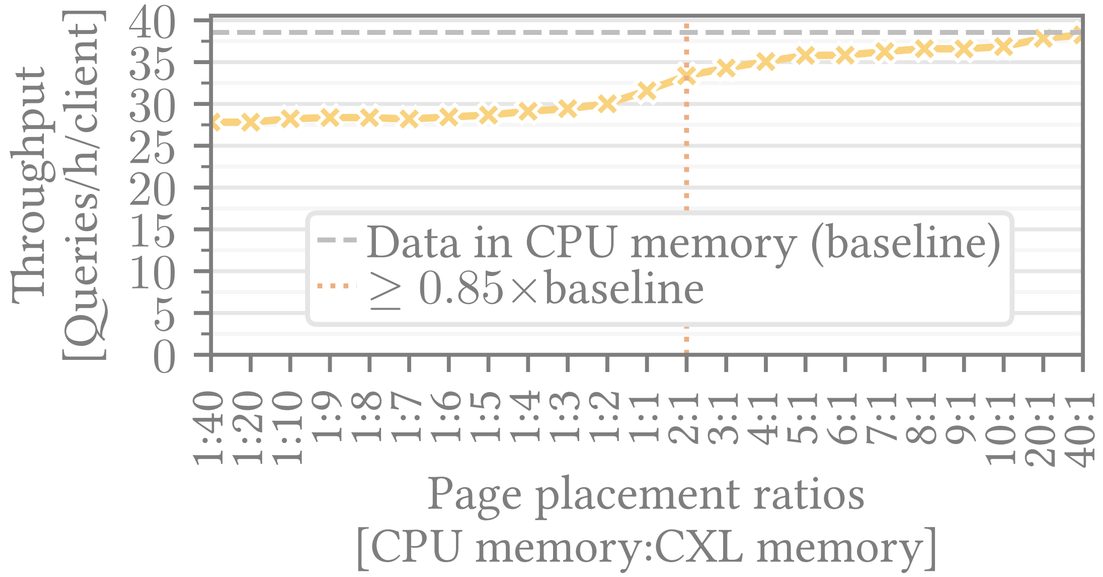
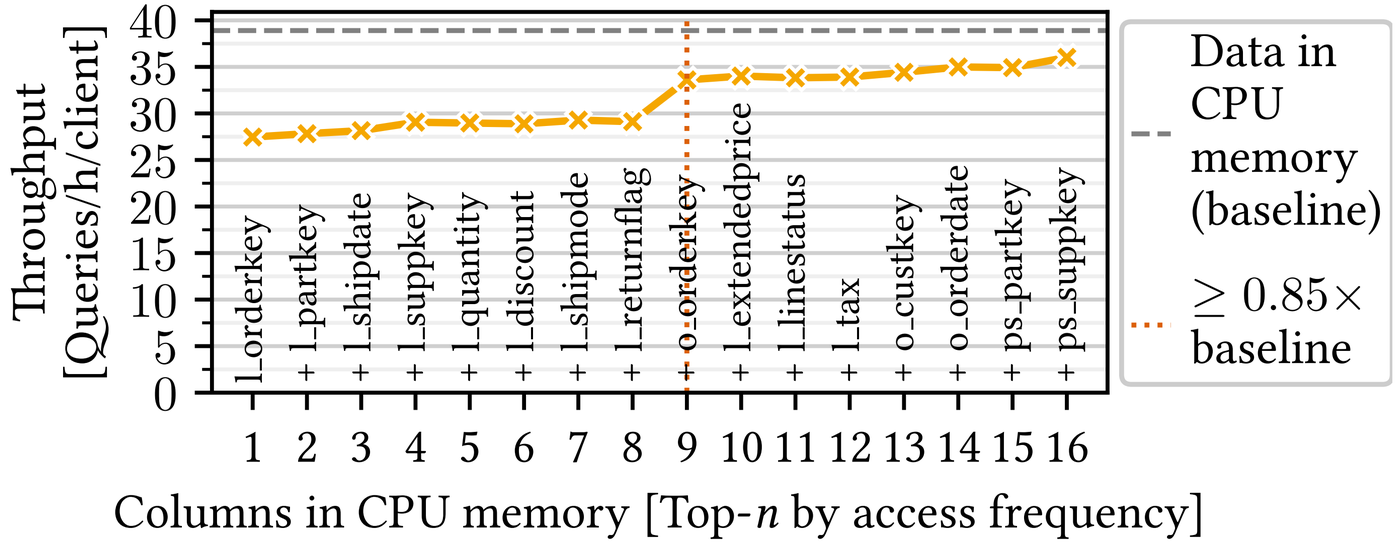


Access Frequency-Based (Column Granularity)



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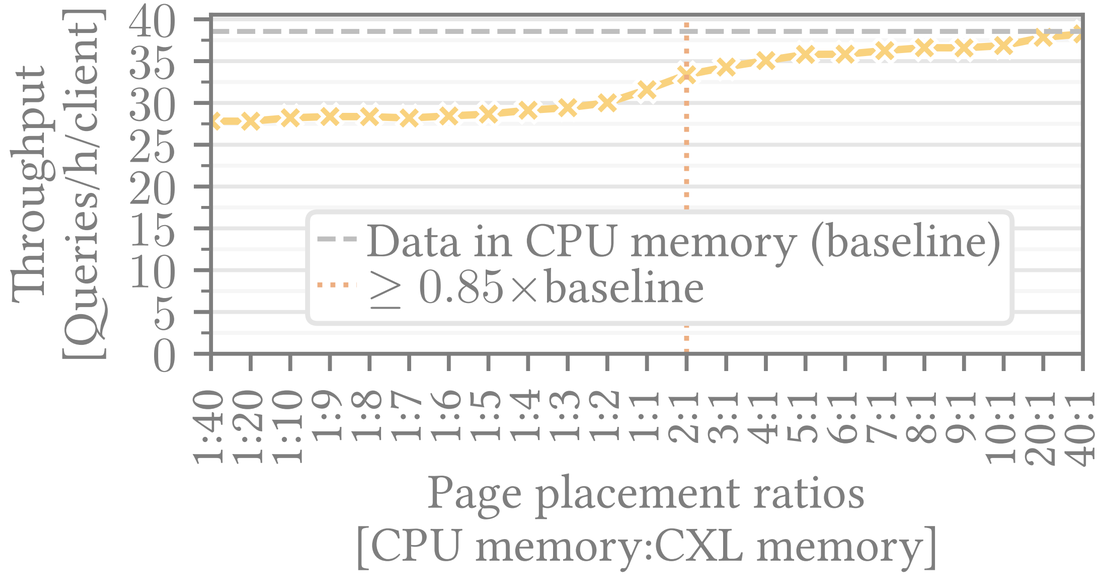

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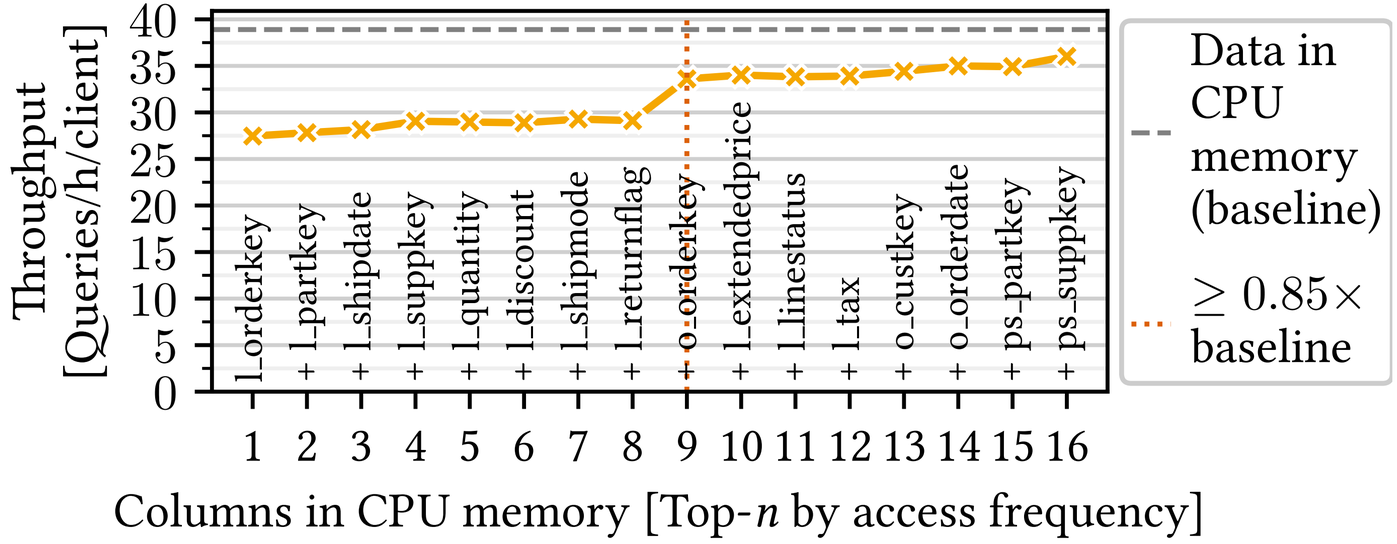

- Accumulate data accesses per column
- Columns with top-n access counts in CPU memory

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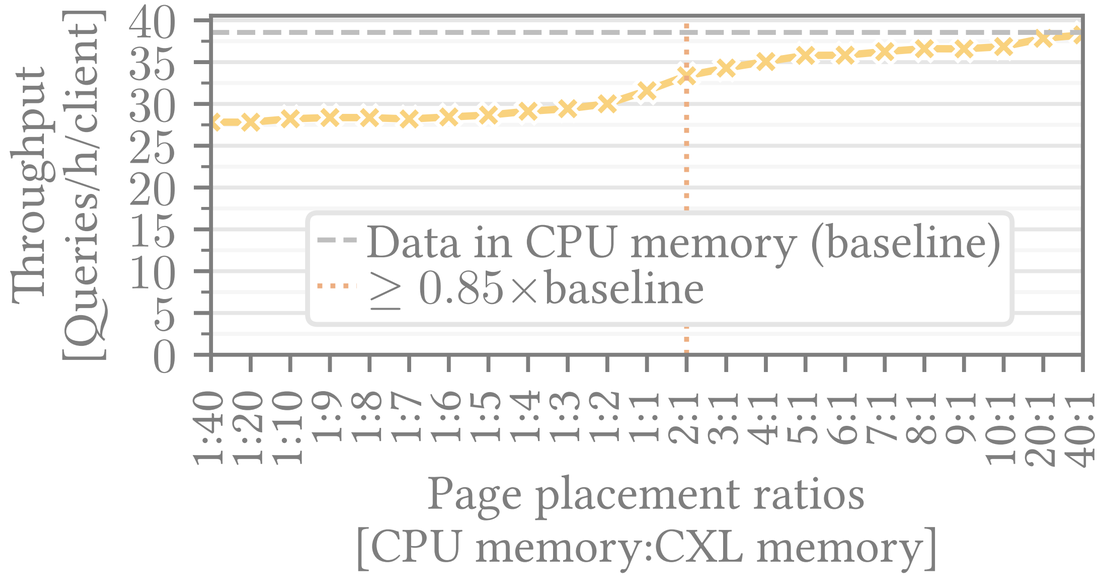

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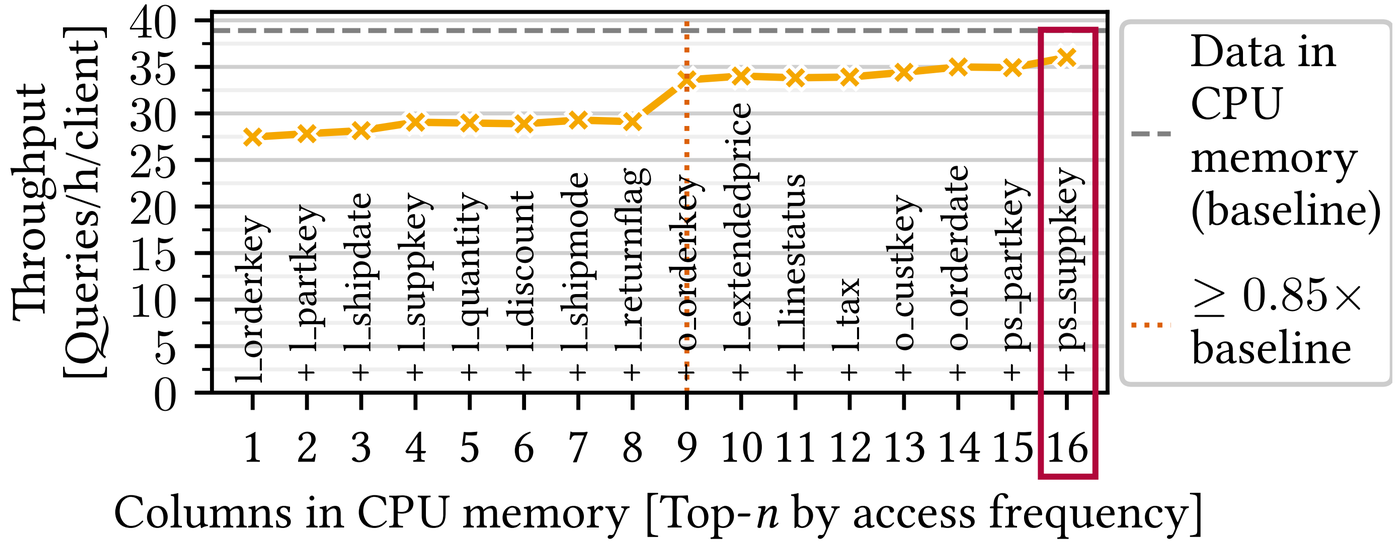

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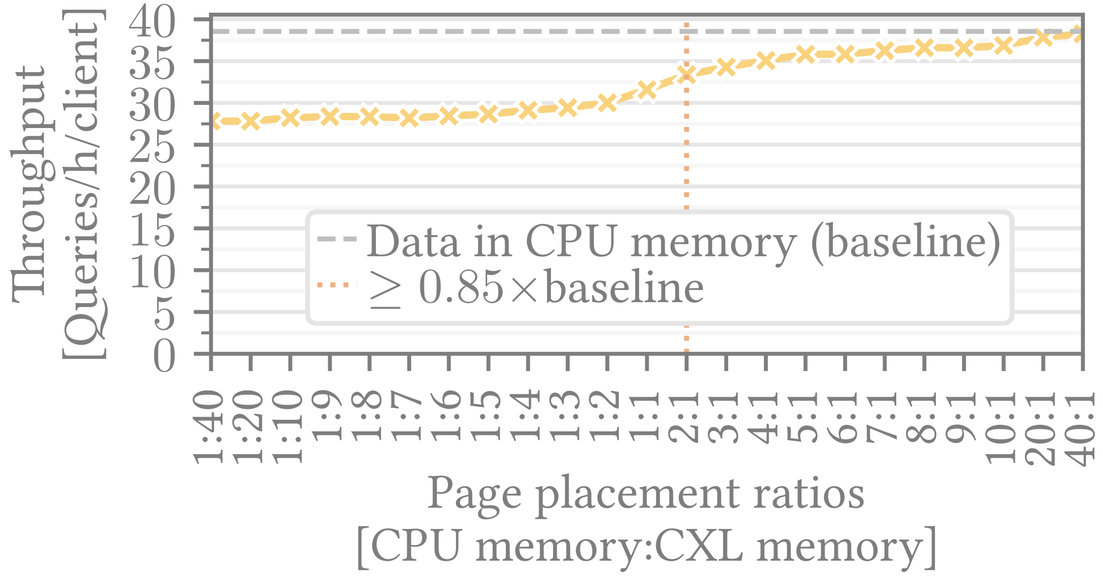

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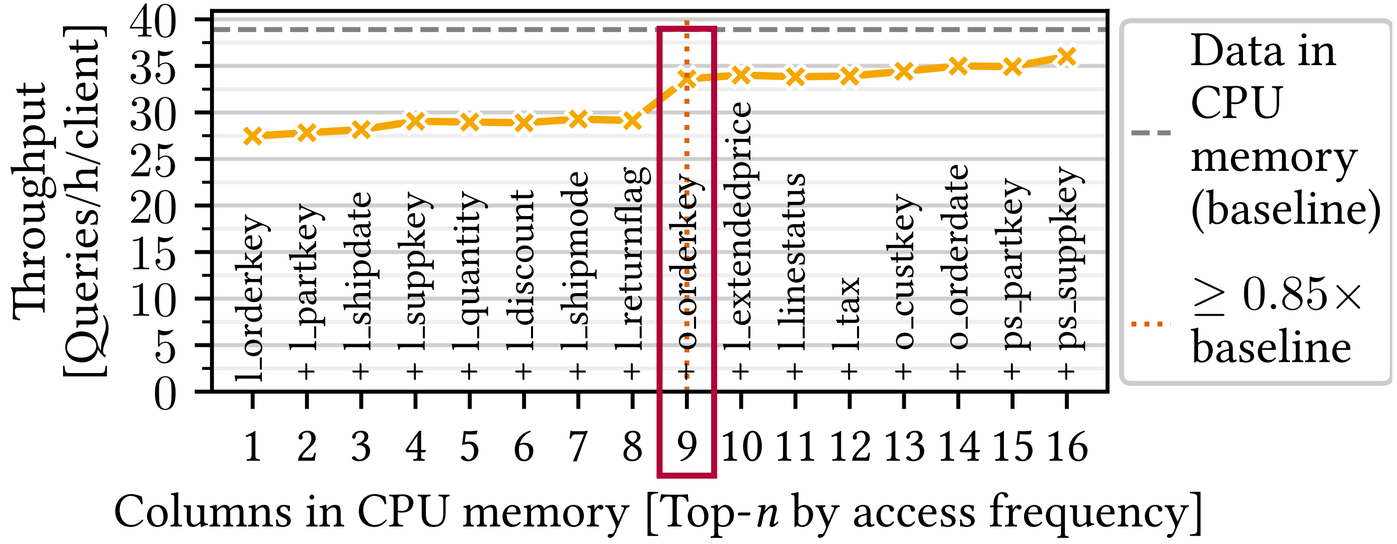

- Accumulate data accesses per column
- Columns with top-n access counts in CPU memory
- Top-16 (23% of table data size) in CPU memory results in 94% baseline performance
- Top-9 (16%) results in 87% baseline performance

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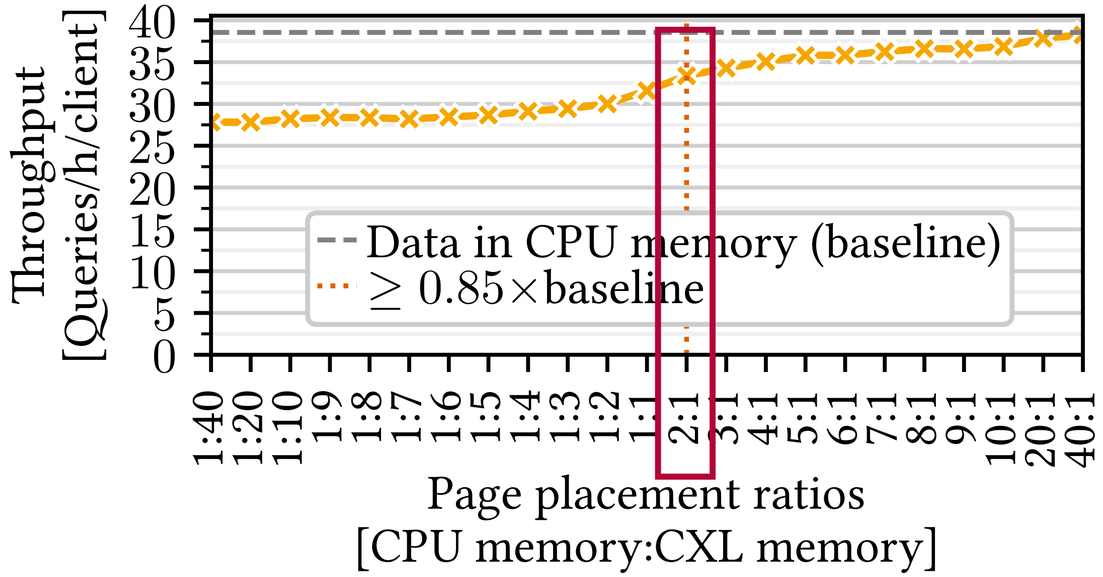

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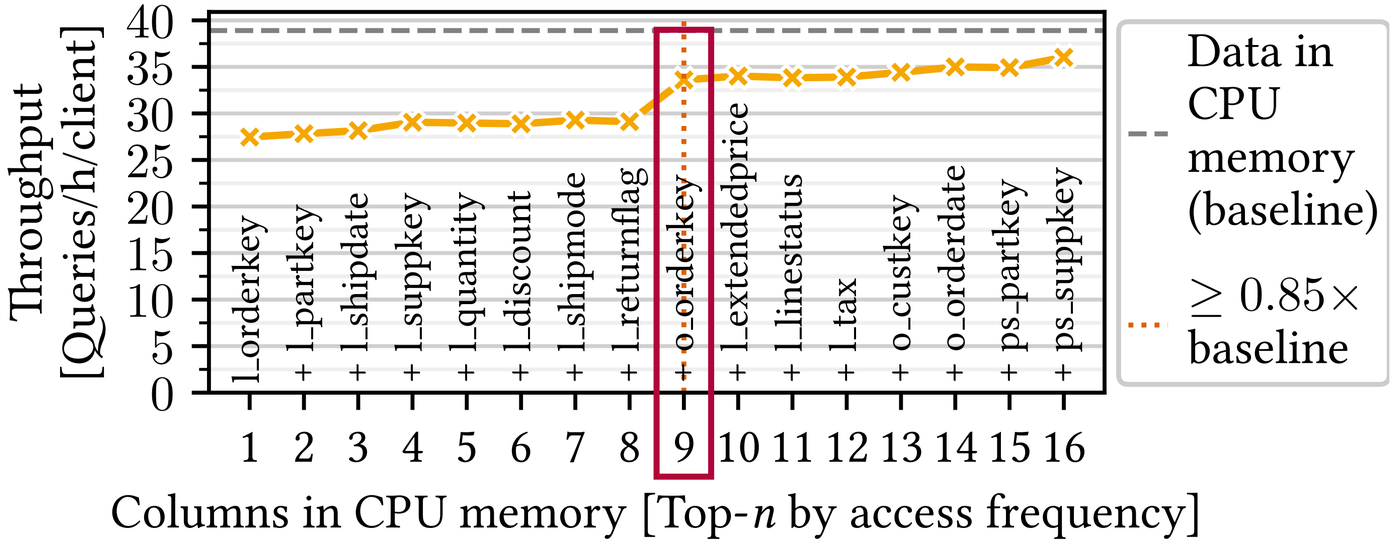

33% in CXL

vs.

84% in CXL

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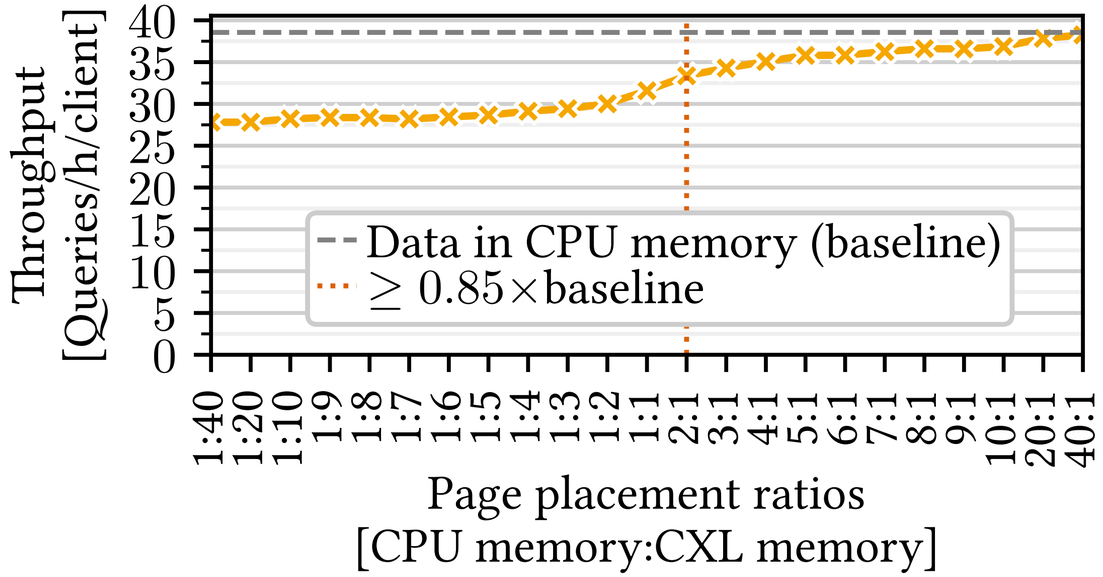

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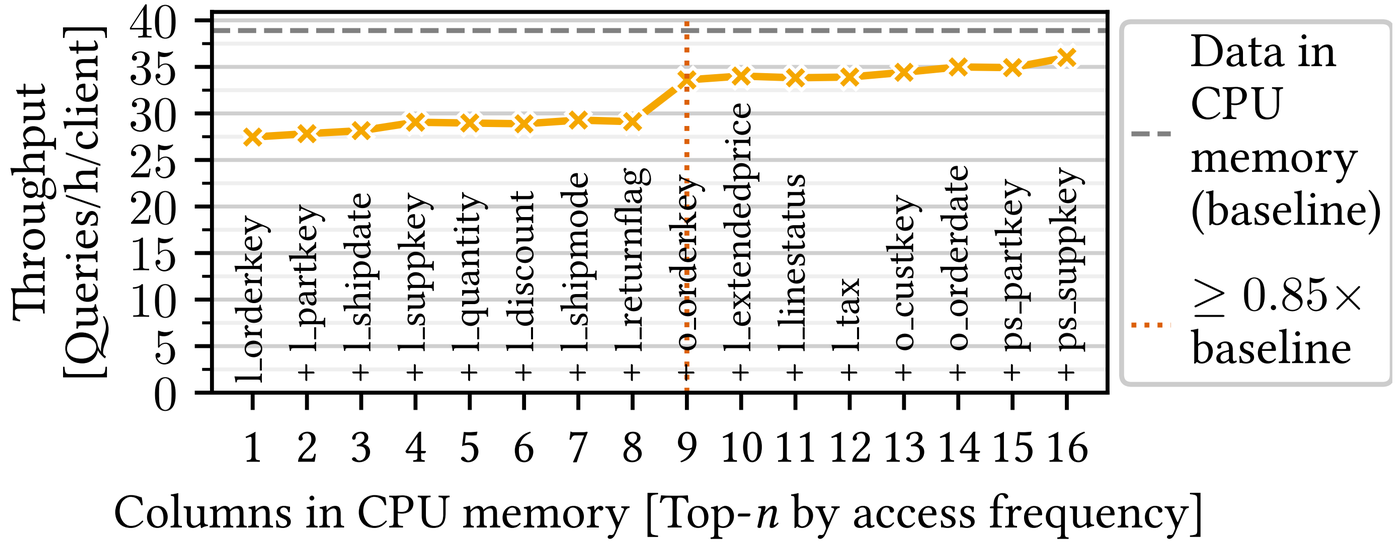

Conclusion

CXL memory for cold and warm data with hot data in CPU memory can lead to high performance when a DBMS uses both CPU and CXL memory.

Economic Viability

Calculate expenses of CPUs and memory DIMMs.

We collected prices of NEMIX DDR4/DDR5 288-PIN RDIMMs on NewEgg.com in March 2025.

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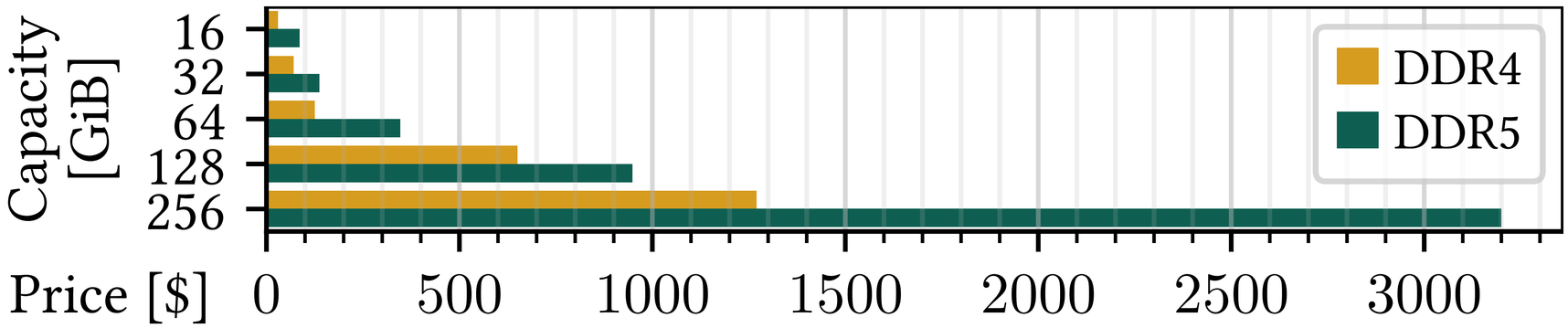

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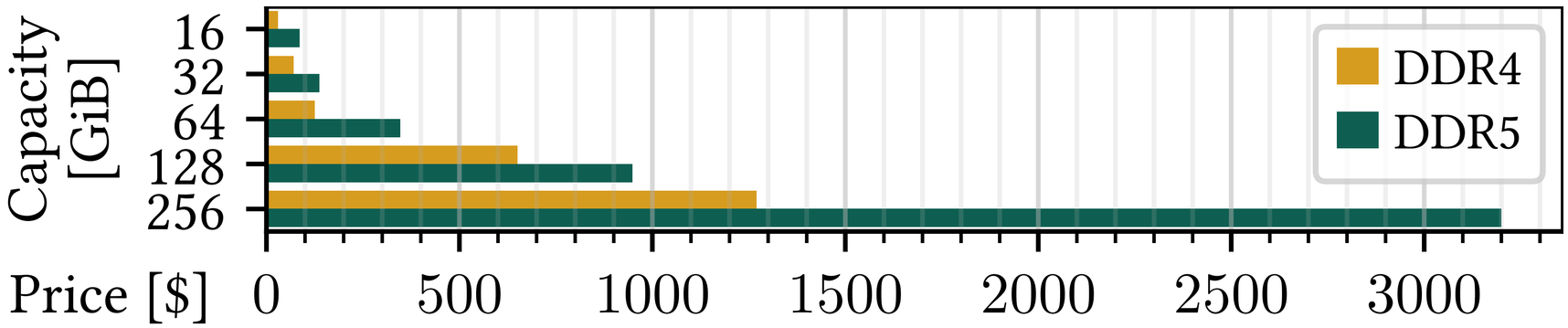

Price [$] per GiB	
DDR4	DDR5
1.9	5.3
2.2	4.3
2.0	5.4
5.1	**7.4**
5.0	**12.5**

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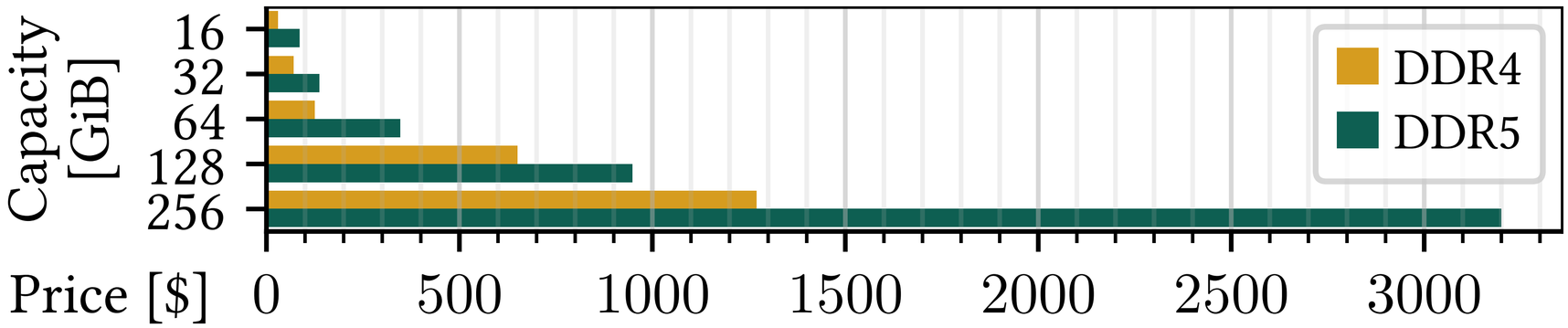

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DDR4	DDR5
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5.1	**7.4**
5.0	**12.5**

→ Avoid 128 GiB / 256 GiB DIMMs to minimize memory expenses.

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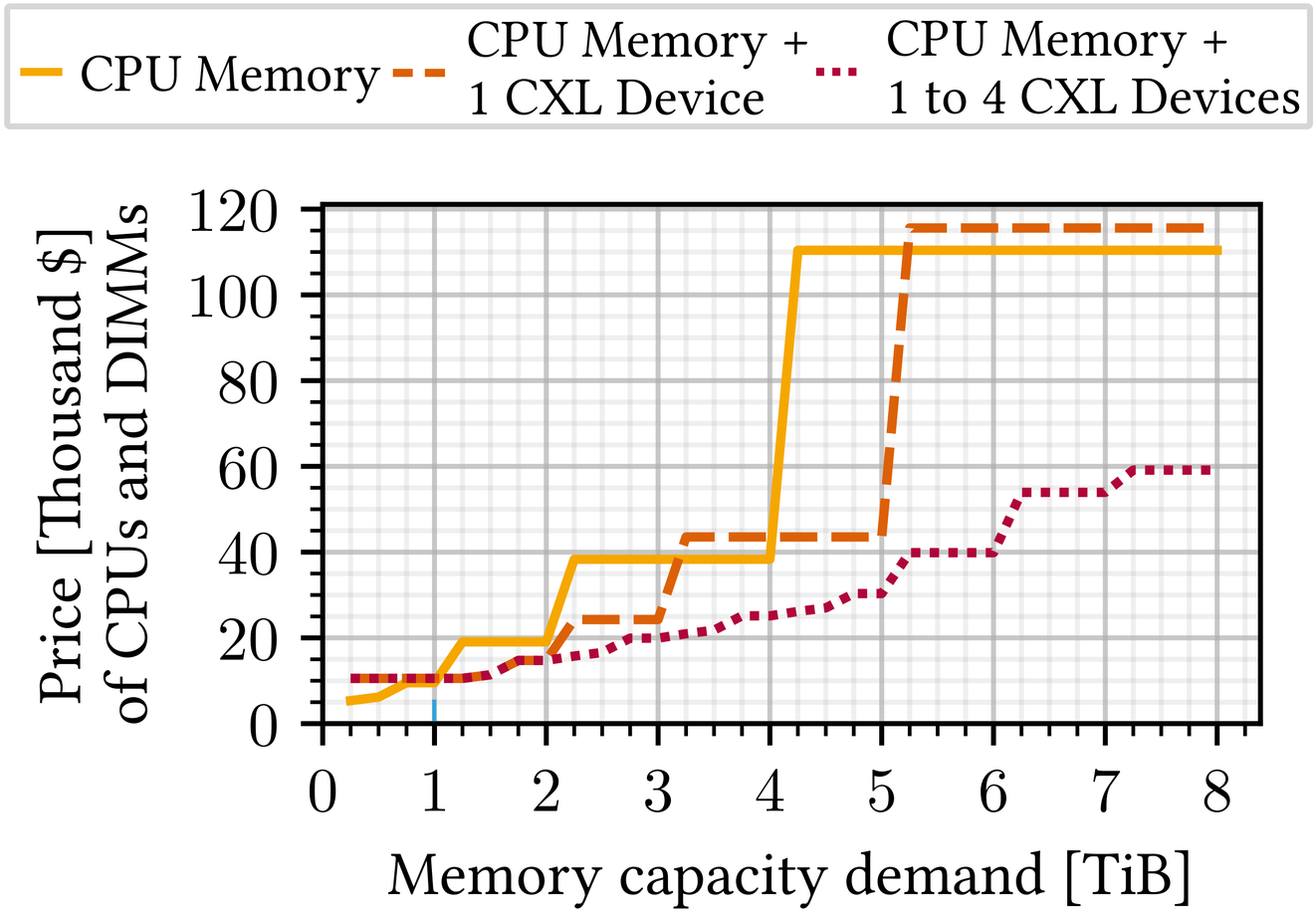

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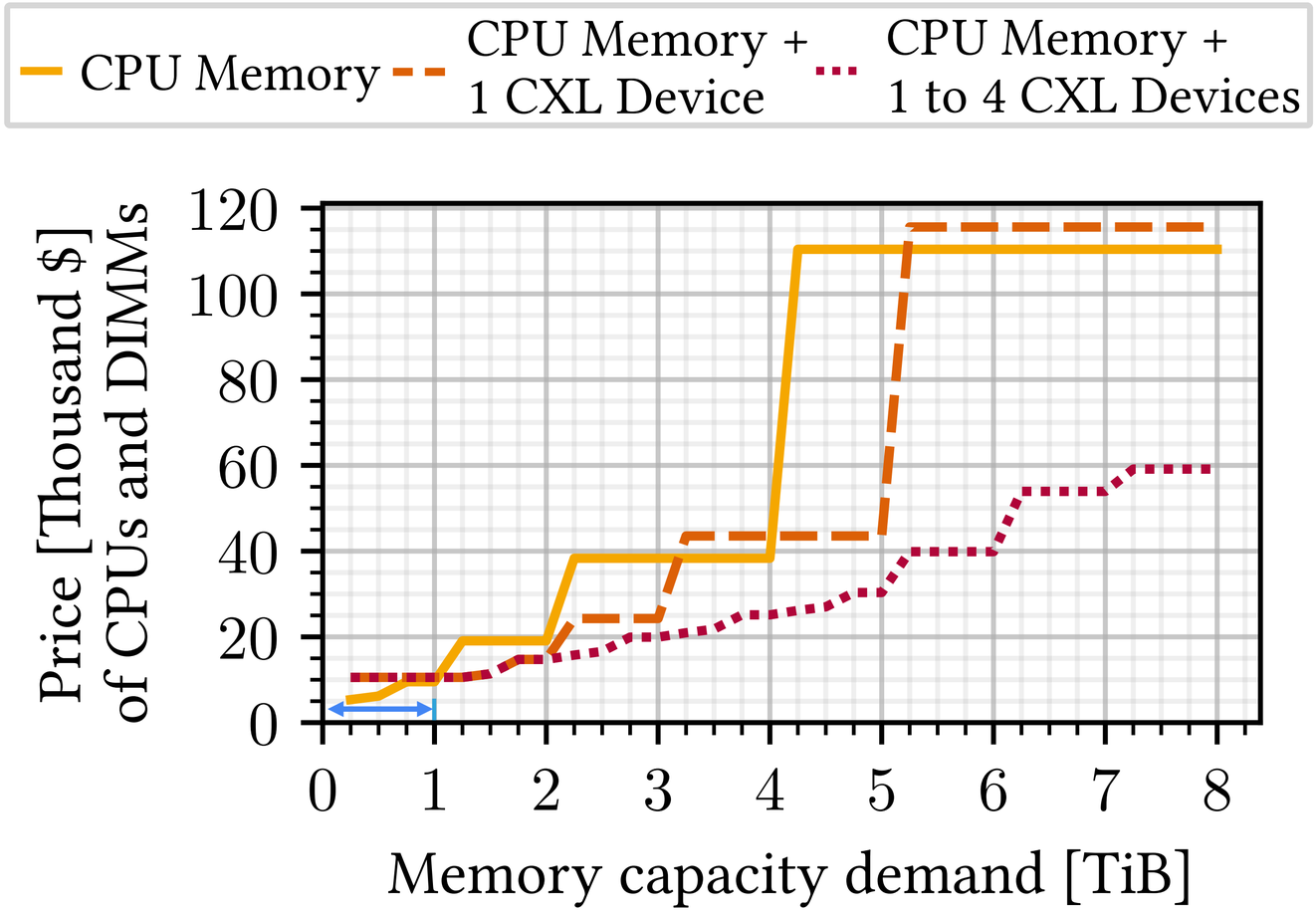
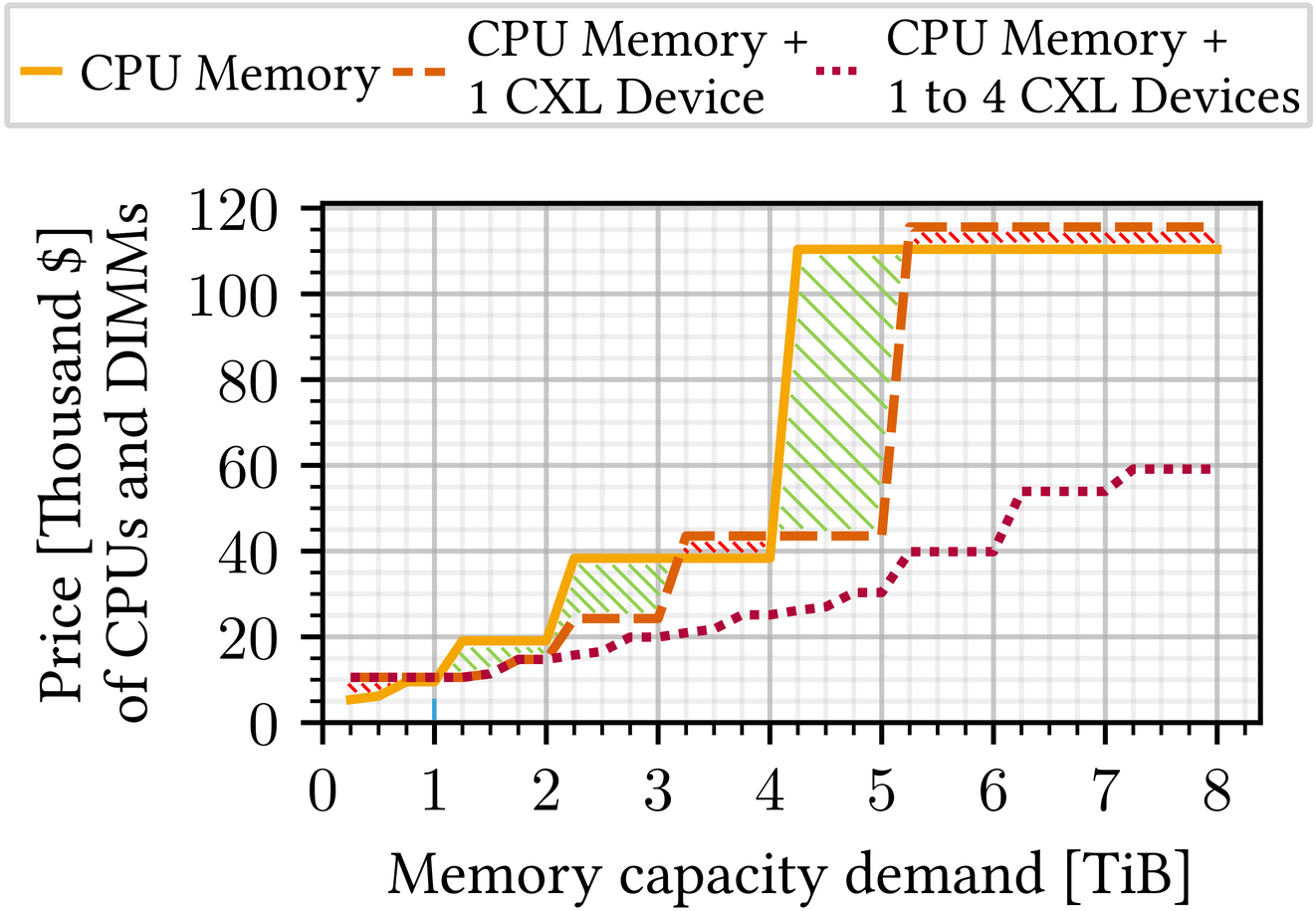


Observations

CPU memory cheapest for demand (D) ≤ 1 TiB.

Economic Viability



Observations

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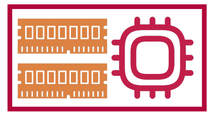

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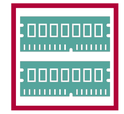
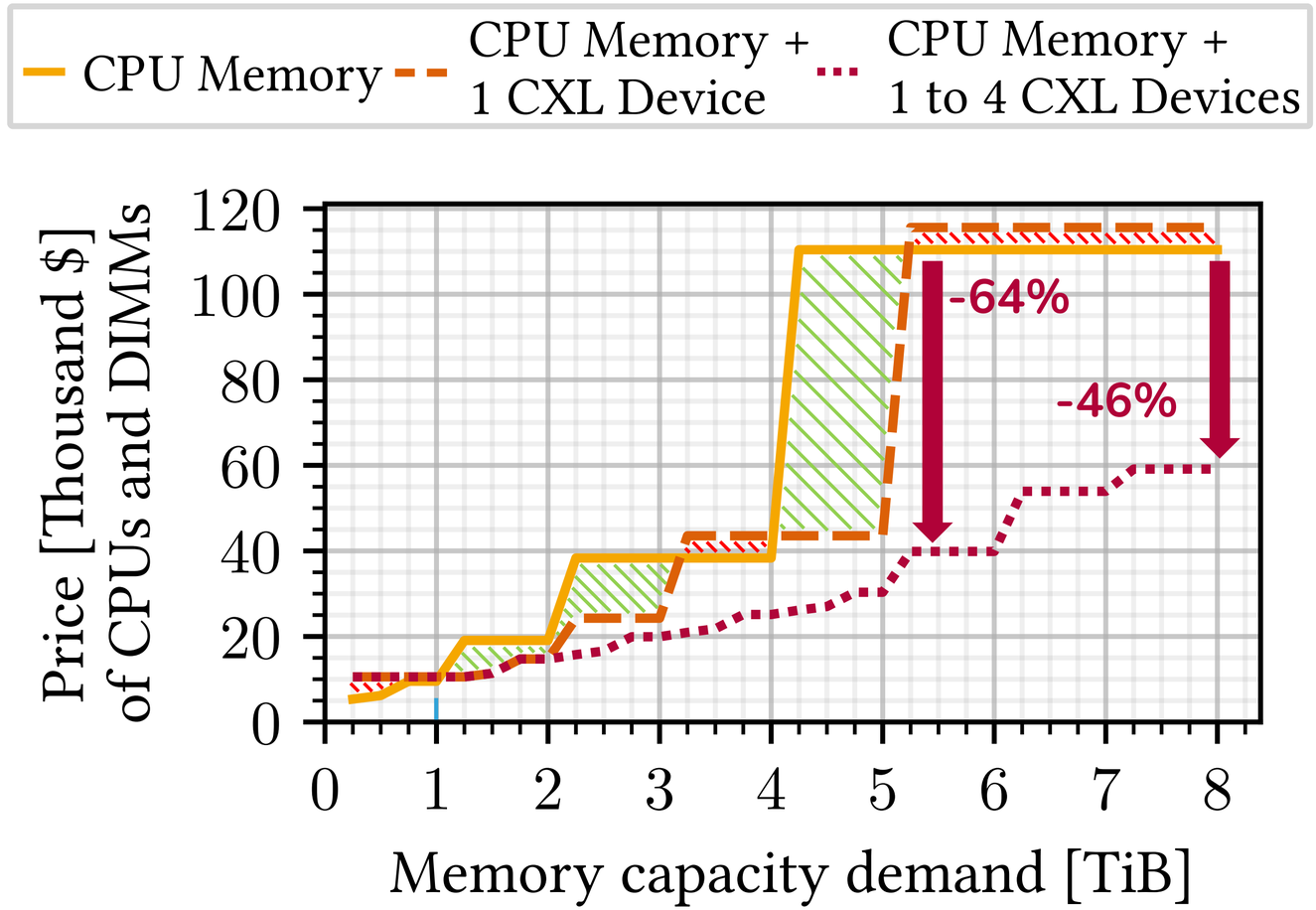


+ 1 device

Economic Viability



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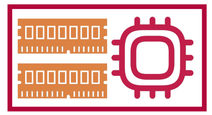

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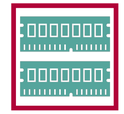

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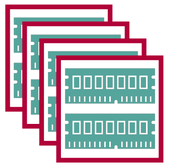
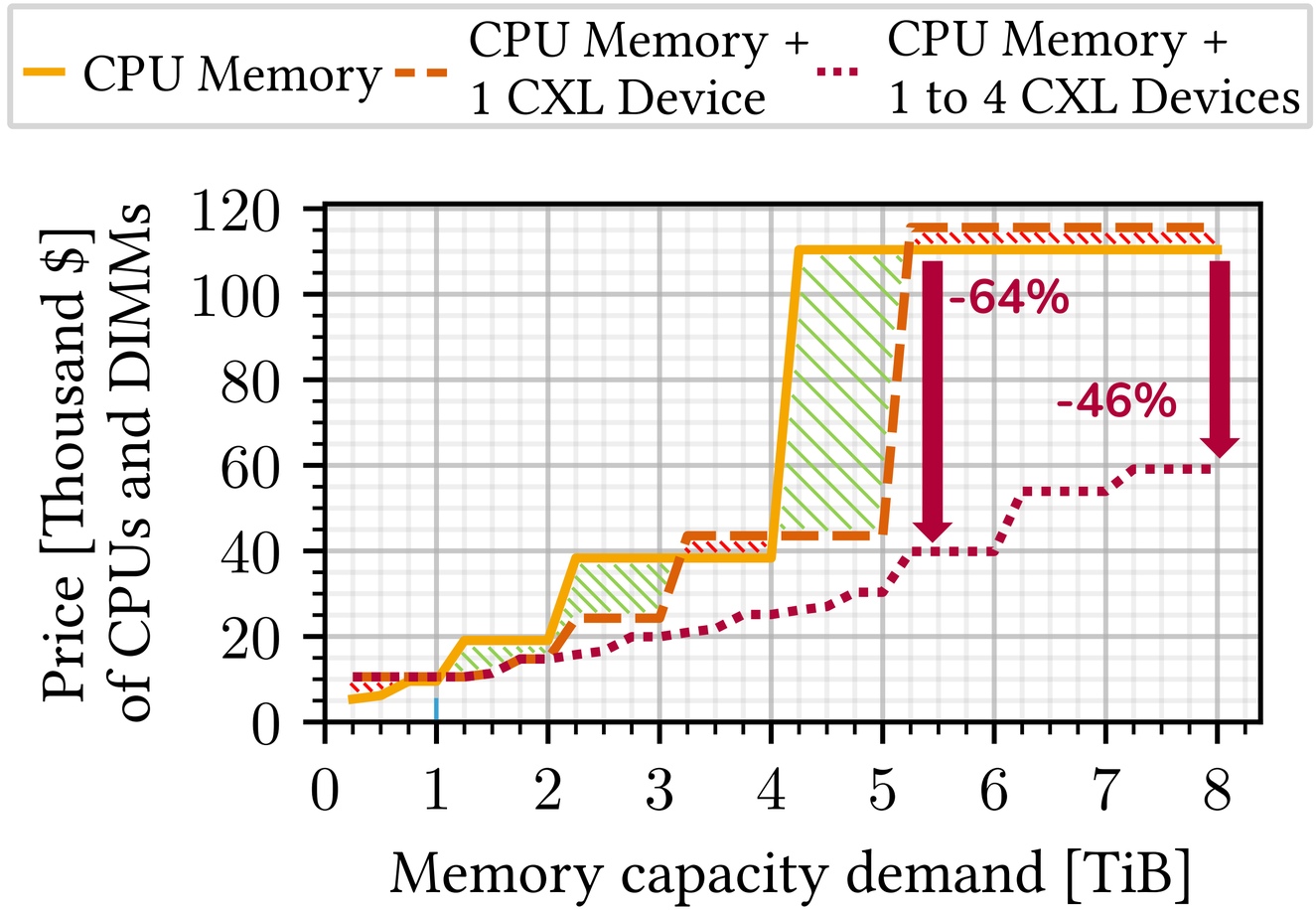


+ 1 to 4 devices

Economic Viability



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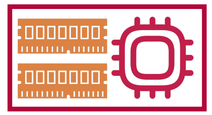

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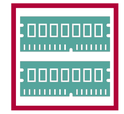

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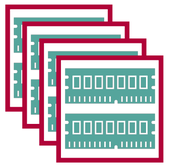

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Reusing DIMMs of old servers further reduces cost of CXL setups.

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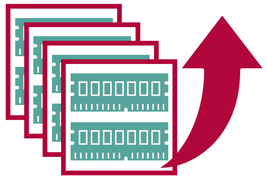

Bandwidth-bound workloads benefit from CXL memory bandwidth of multiple devices.

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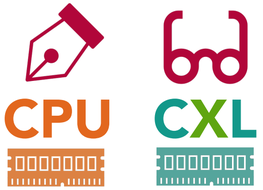

Write-throughput limited workloads can benefit from writes to CPU memory and reads from CXL memory.

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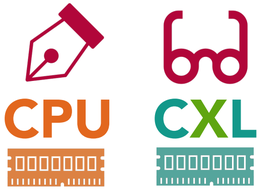
Bandwidth-bound workloads benefit from CXL memory bandwidth of multiple devices.



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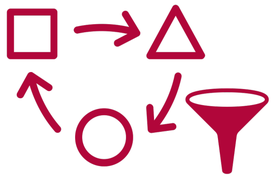
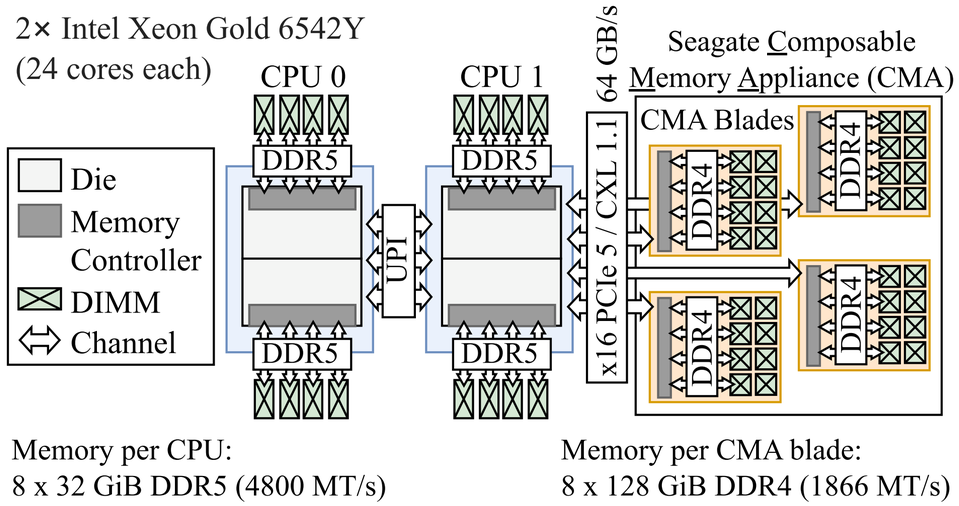
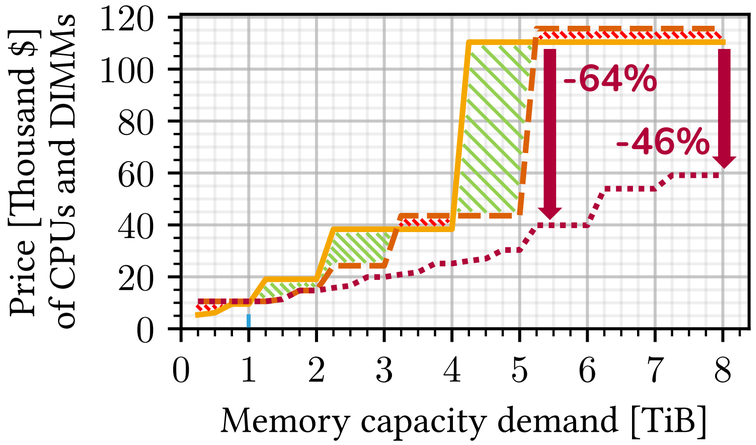
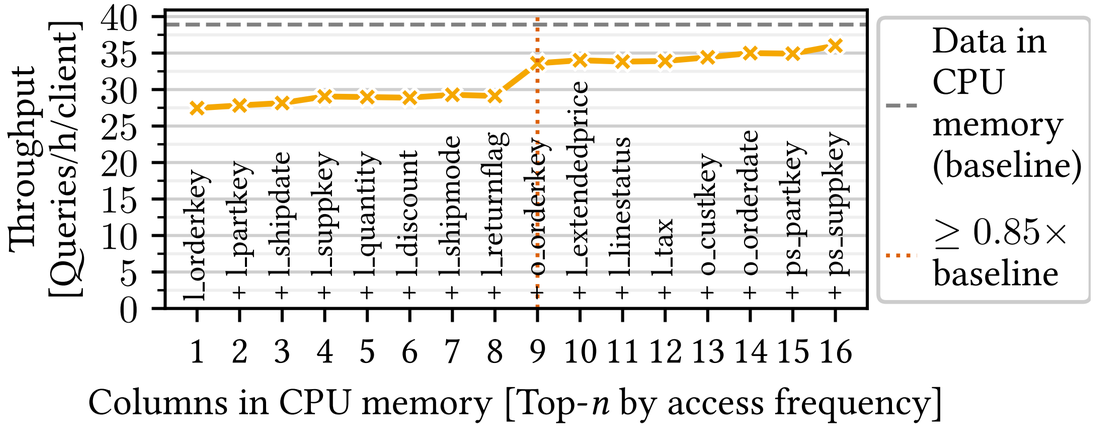


Changing data structures according to their memory bottleneck improves performance.







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Contact

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weisgut.com

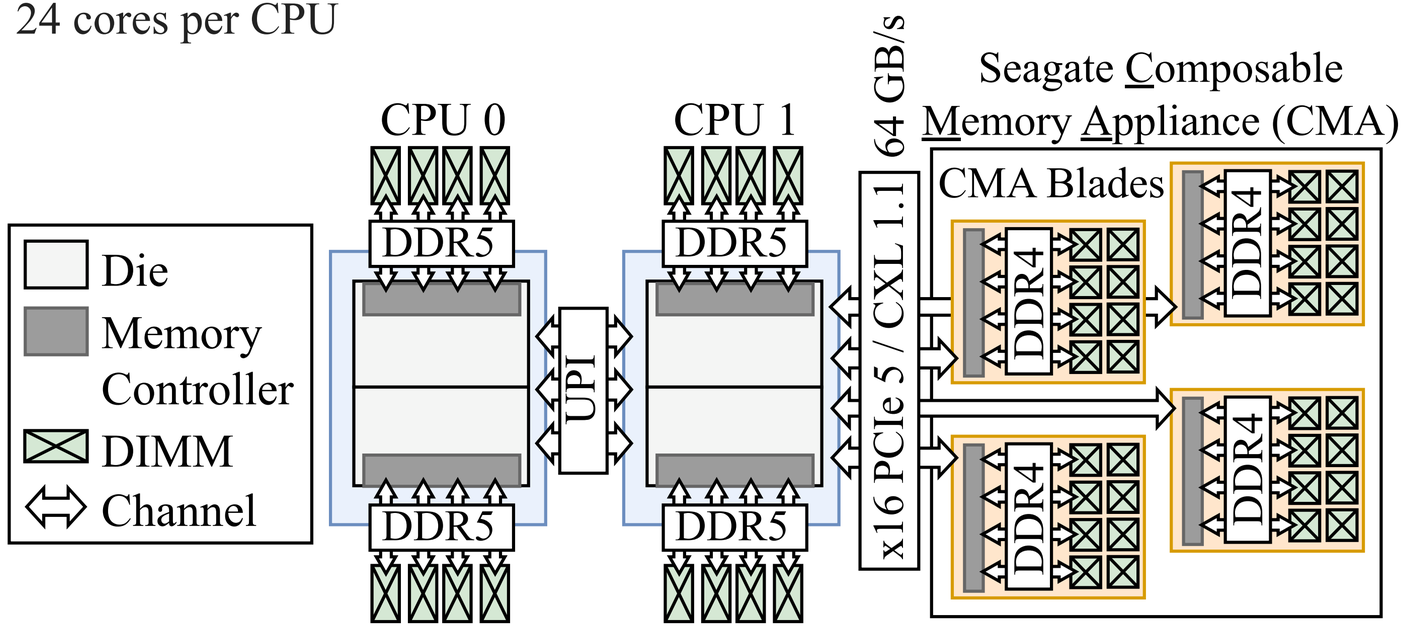
Data Engineering Systems Group @ HPI

hpi.de/rabl

BACKUP

Hardware Setup

2× Intel Xeon Gold 6542Y (Emerald Rapids)
24 cores per CPU

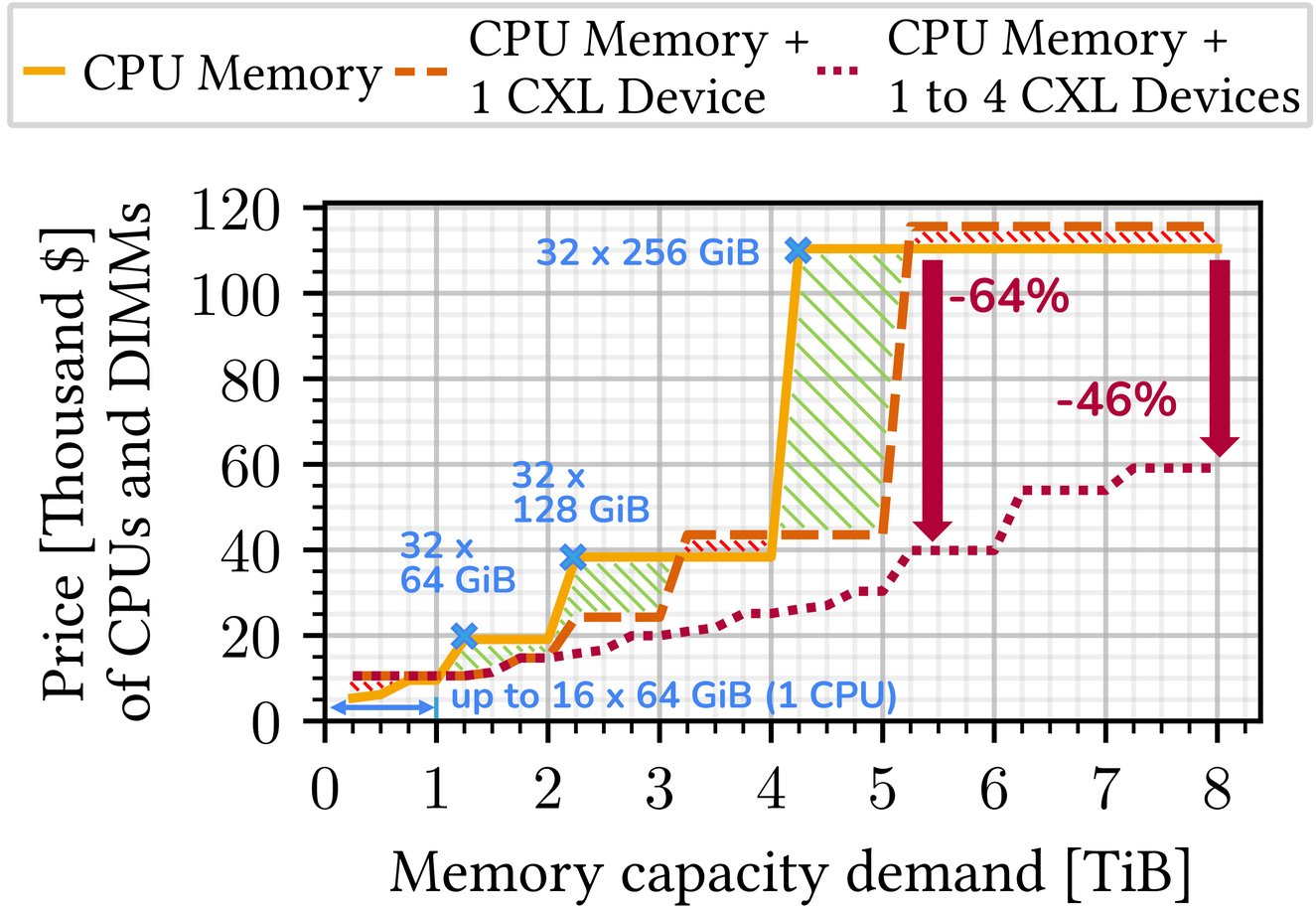


Memory per CPU:
8 x 32 GiB DDR5 (4800 MT/s)

Memory per CMA blade:
8 x 128 GiB DDR4 (1866 MT/s)

Server	Supermicro SYS-741GE-TNRT
CPUs	2 Intel 5th Gen Xeon Scalable Gold 6542Y with 24 cores
Caches	L1i: 32 KiB, L1d: 48 KiB, L2: 2 MiB, L3: 60 MiB
Memory	8 32 GB DDR5 with a speed of 4800 MT/s
OS	Ubuntu 24.04, Kernel 6.13

Economic Viability



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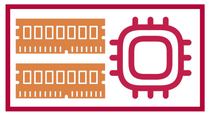

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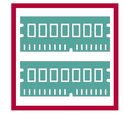

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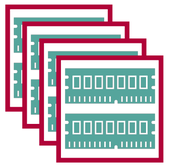

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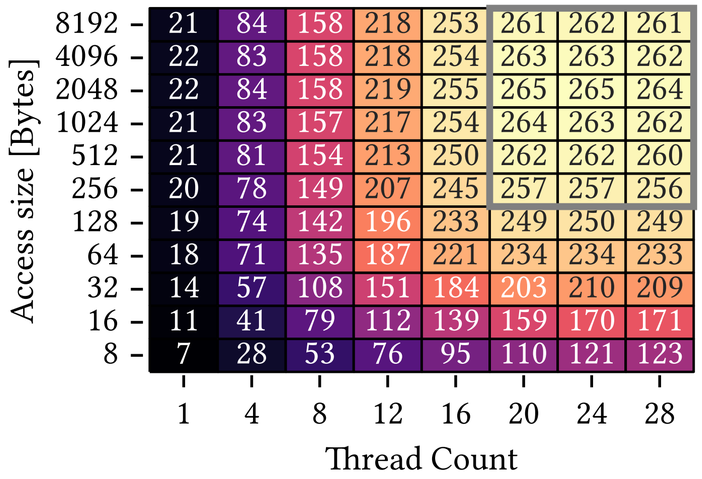
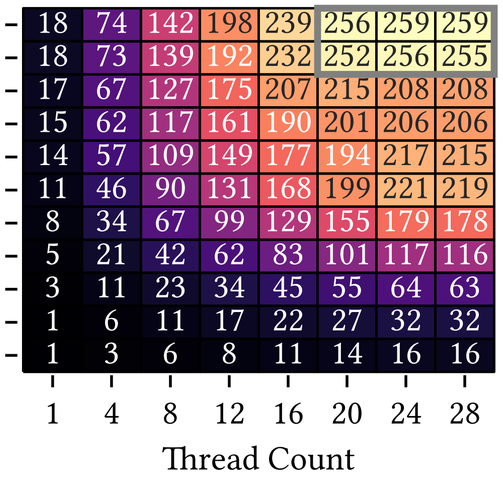
Reusing DIMMs of old servers further reduces cost of CXL setups.

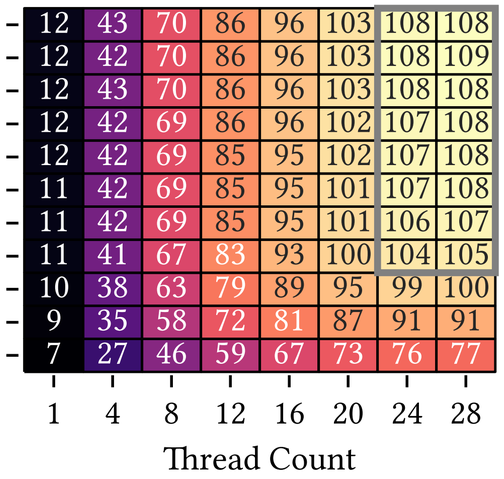
Throughput – CPU Memory & CXL Device Memory



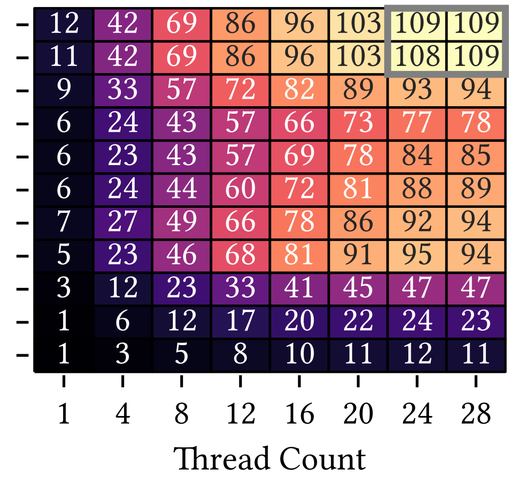
a) Sequential Reads CPU)



b) Random Reads CPU)



c) Sequential Writes CPU)



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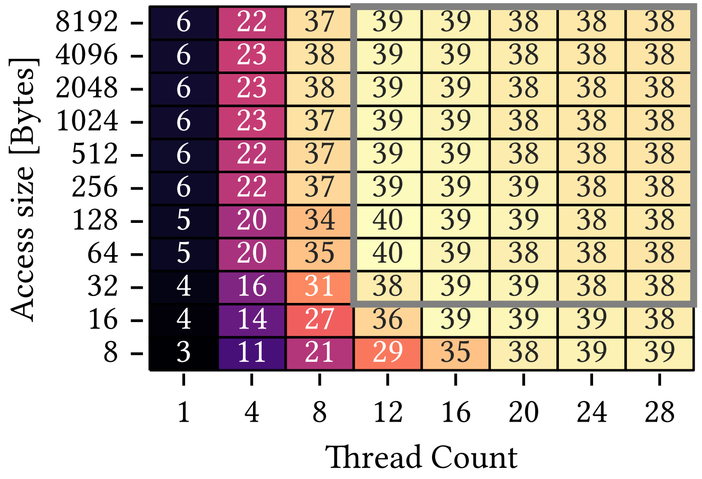
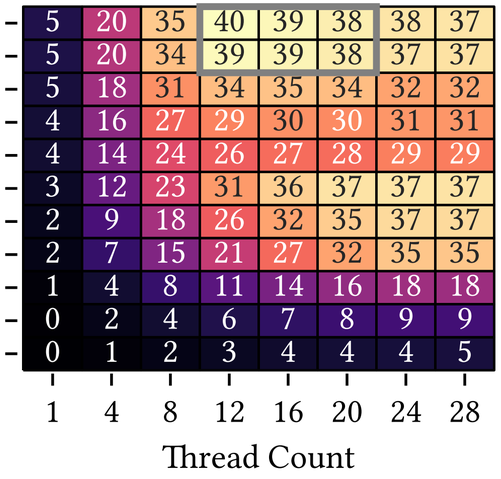


e) Sequential Reads CXL)



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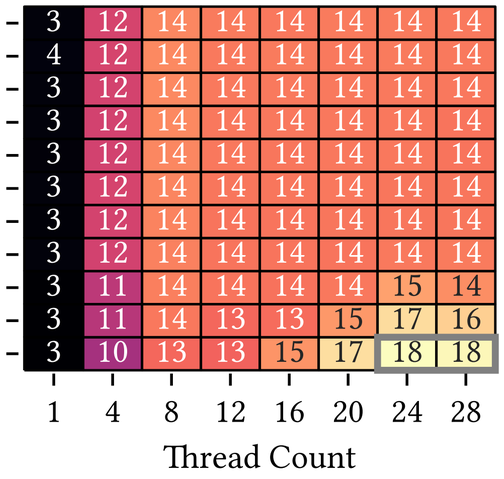

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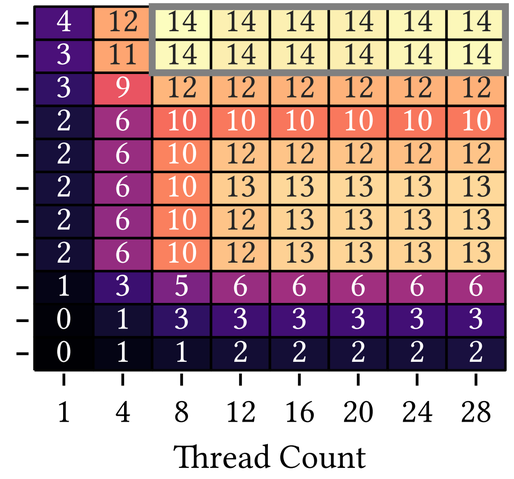
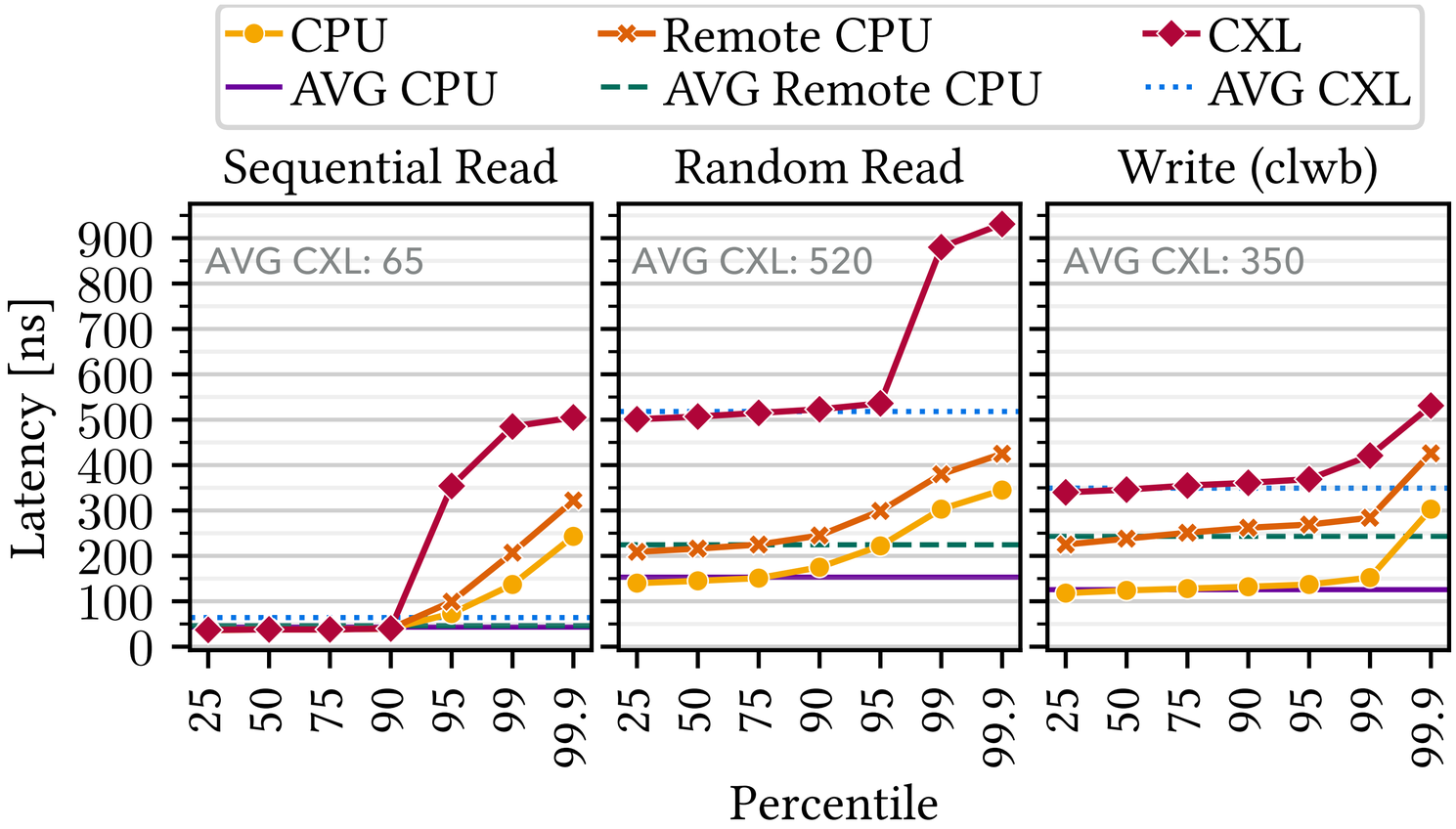


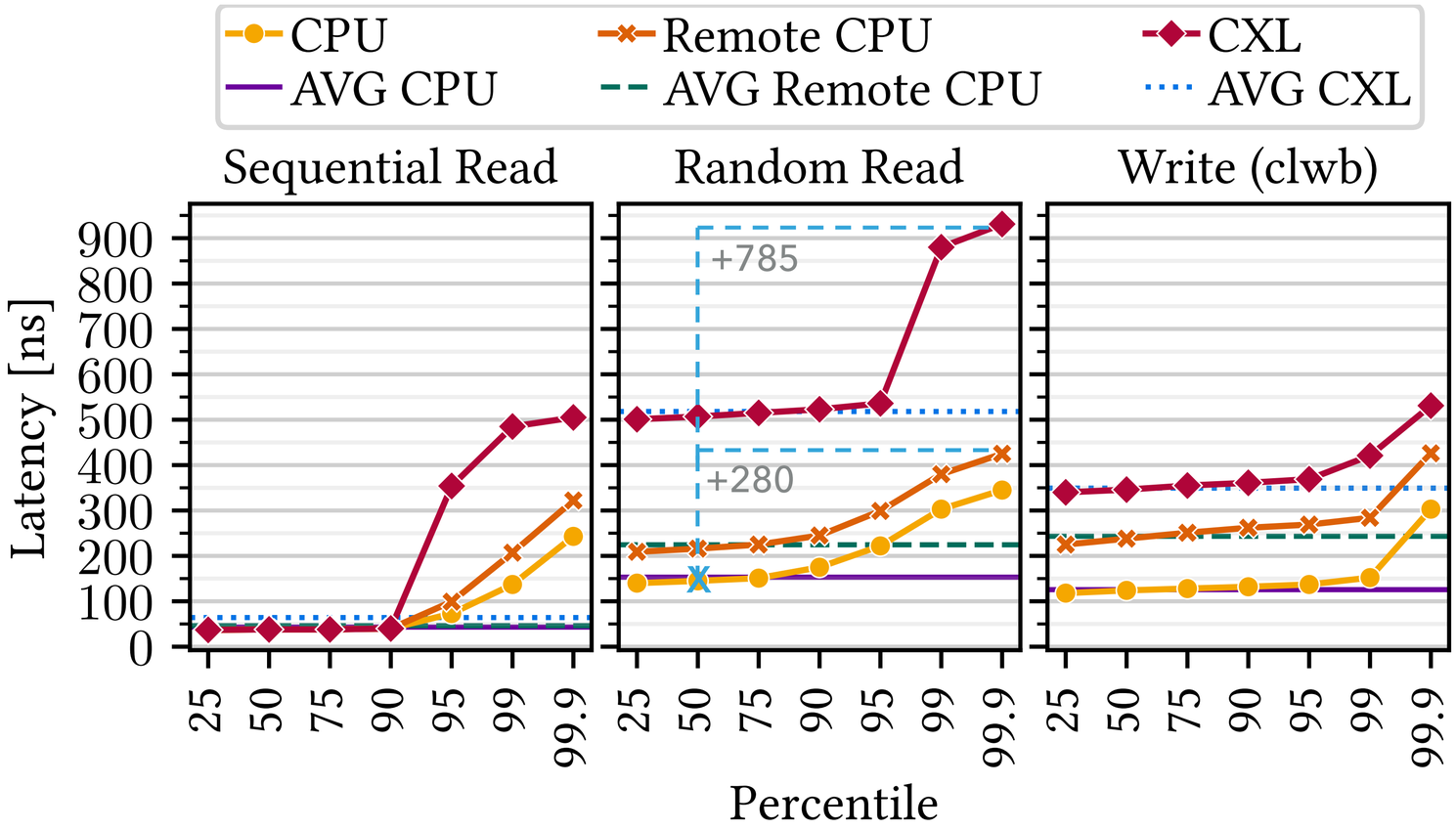
h) Random Writes CXL)

Latency



- 8 B reads/writes
- Reads: load + fence
- Writes: first load cache line, then measure store + clwb + fence

Latency



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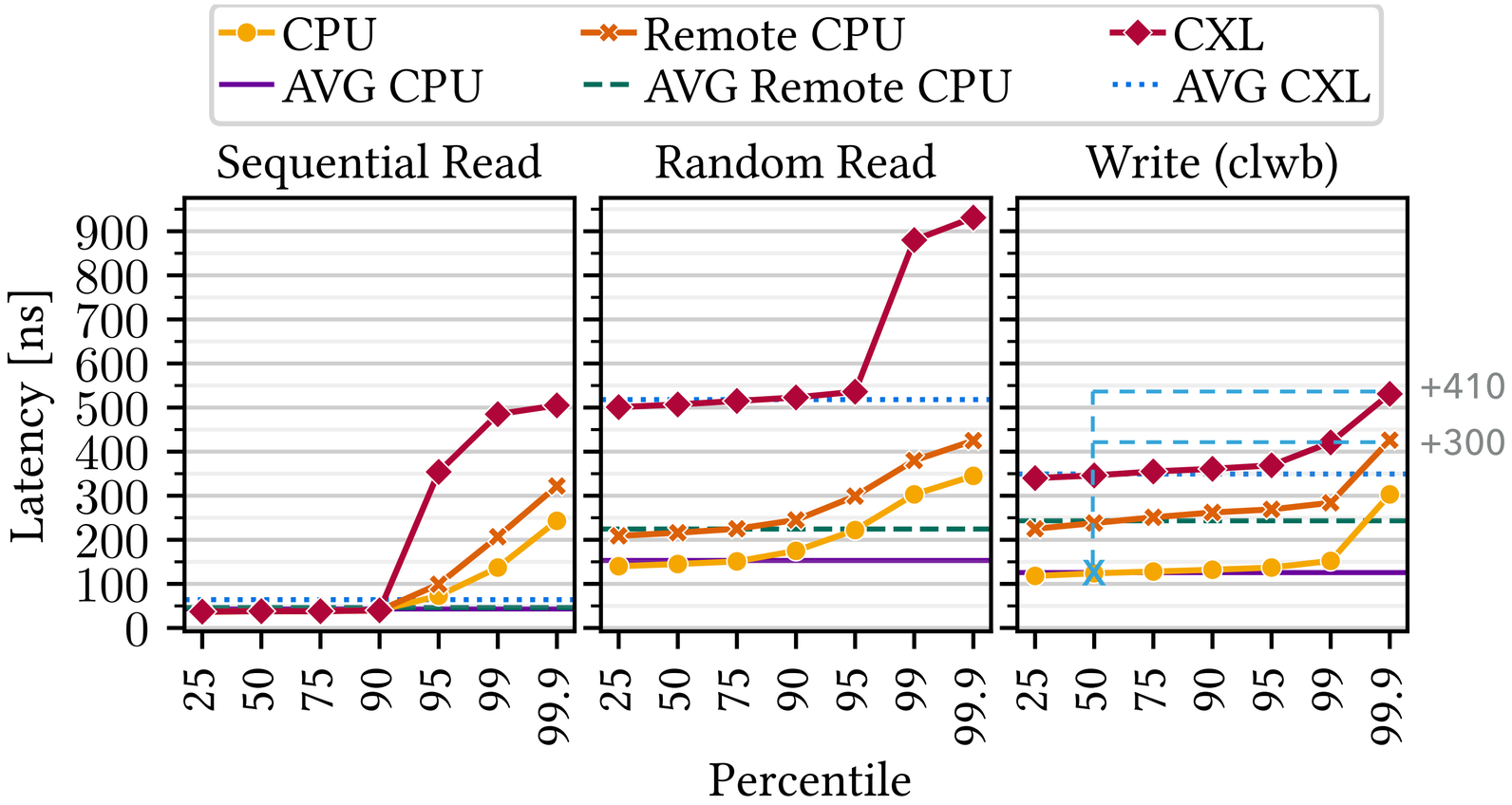

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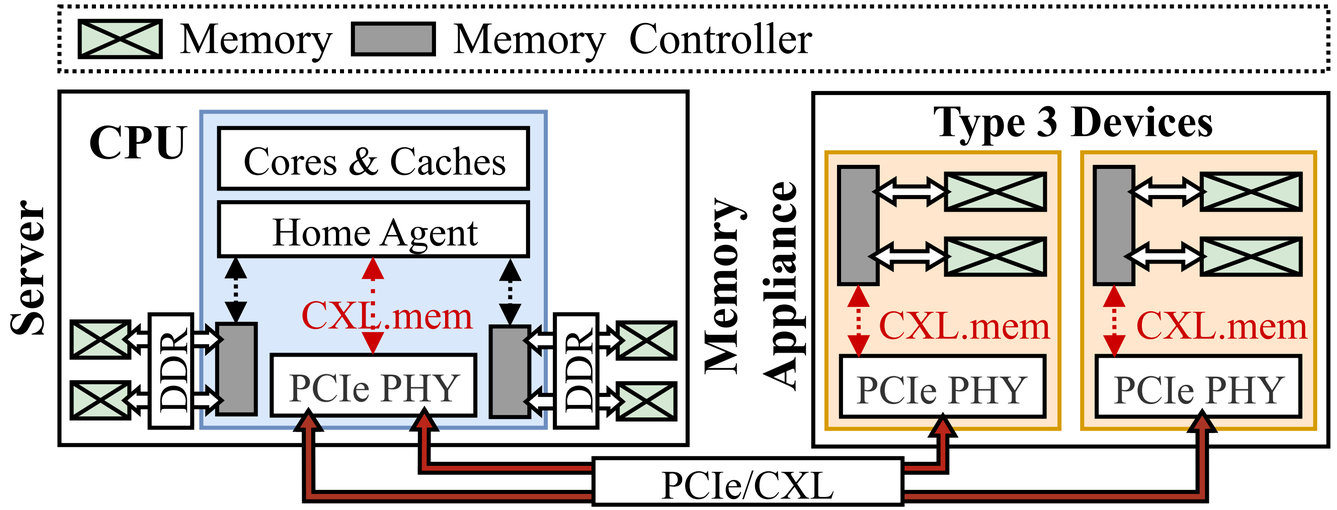
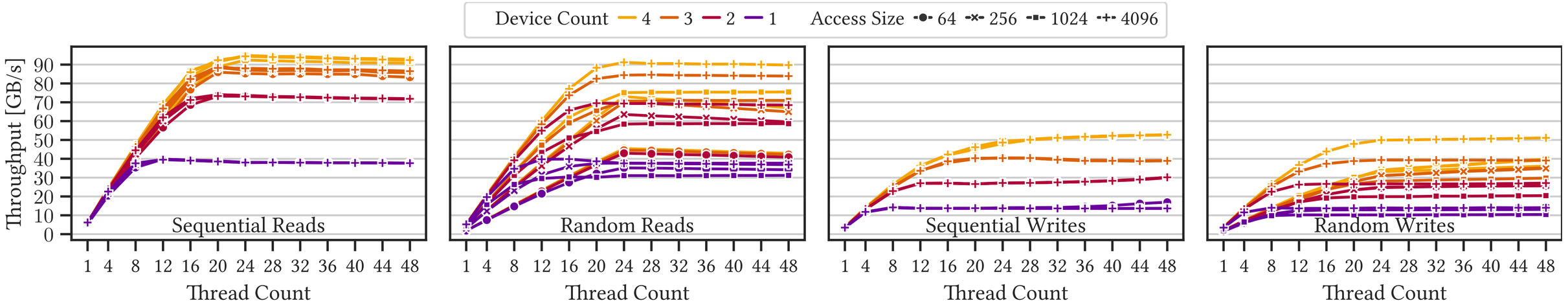
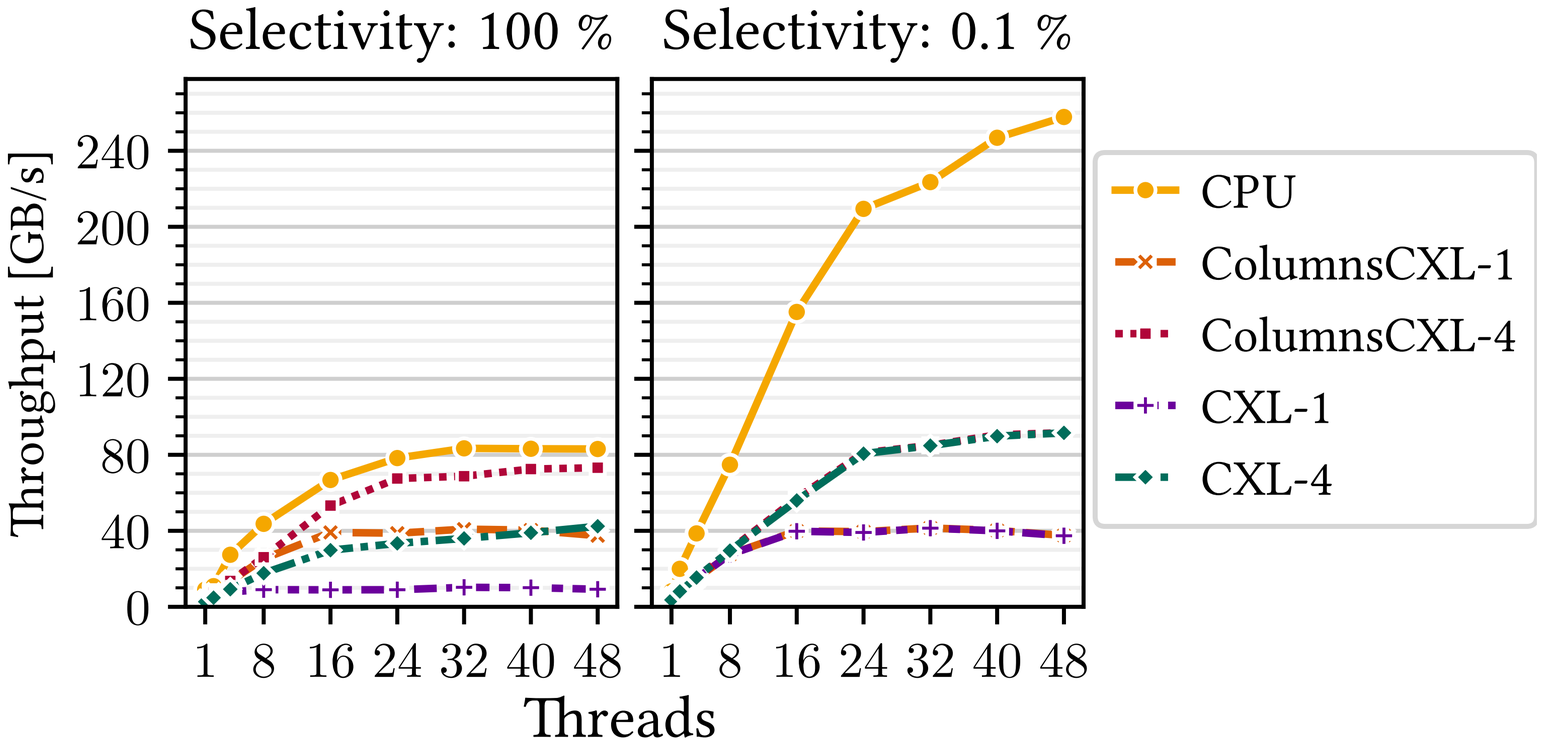
Memory Expansion with Multiple CXL Devices



Throughput – Multiple CXL Devices



In-Memory SIMD Column Scan



- 4-B unsigned integer (uint) values
- Each thread scans separate column (512 MiB, ~134 M values)
- Scan writes 4-B uint tuple identifiers (TIDs) for matches
- Allocate memory region for each column and each TID list

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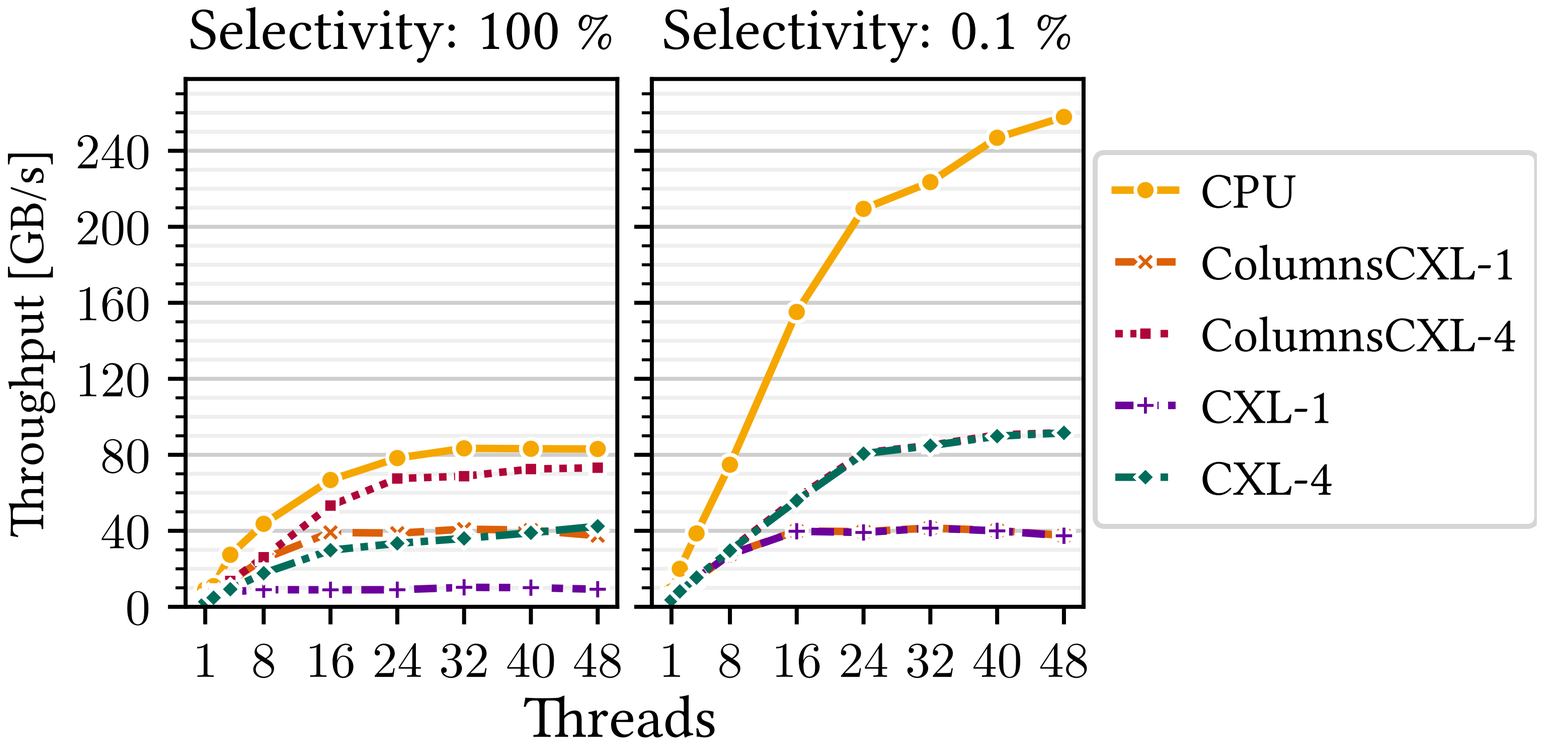

Observations

- Lower selectivity → fewer writes → higher performance
- Write throughput limits scan since it writes a 4-B TID for each read value
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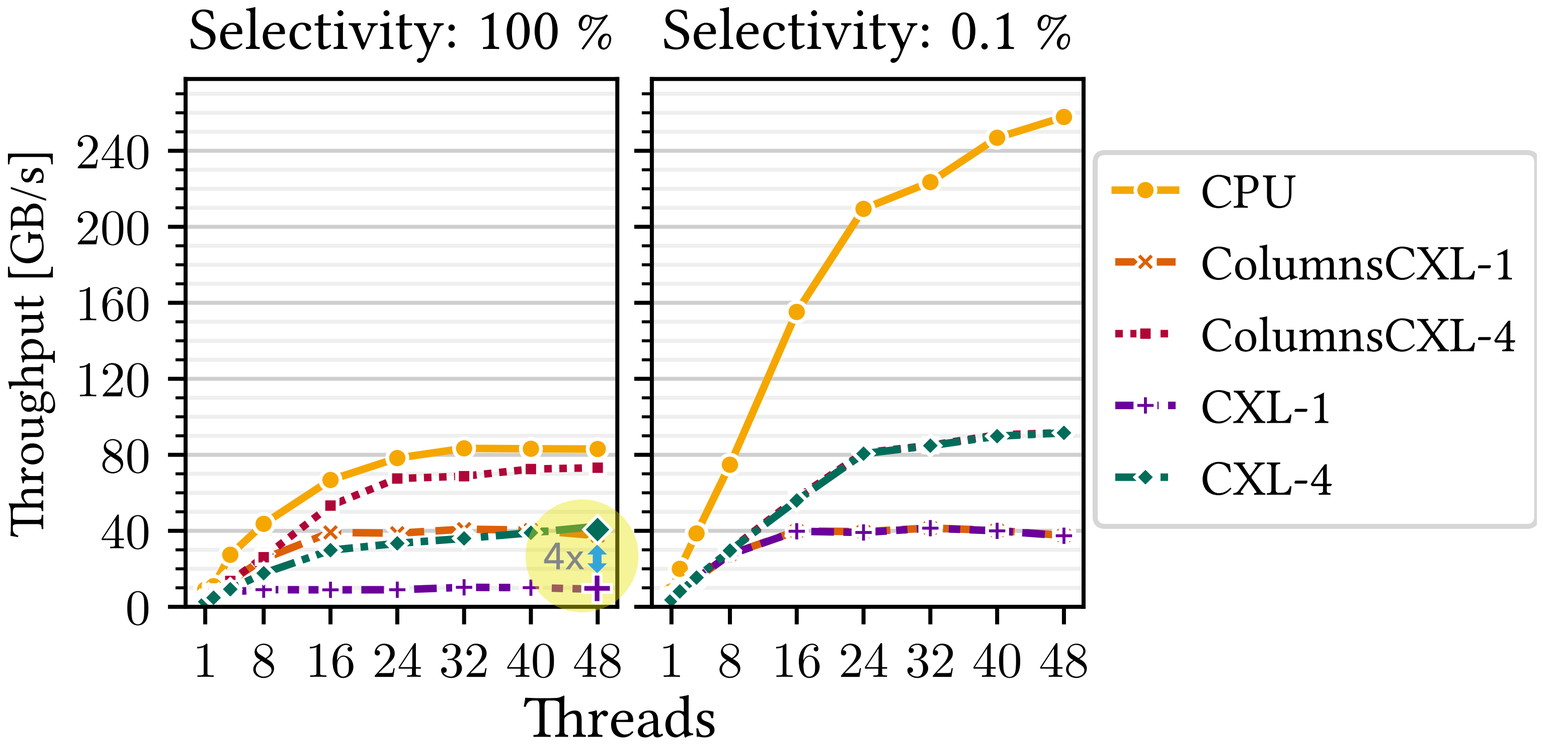

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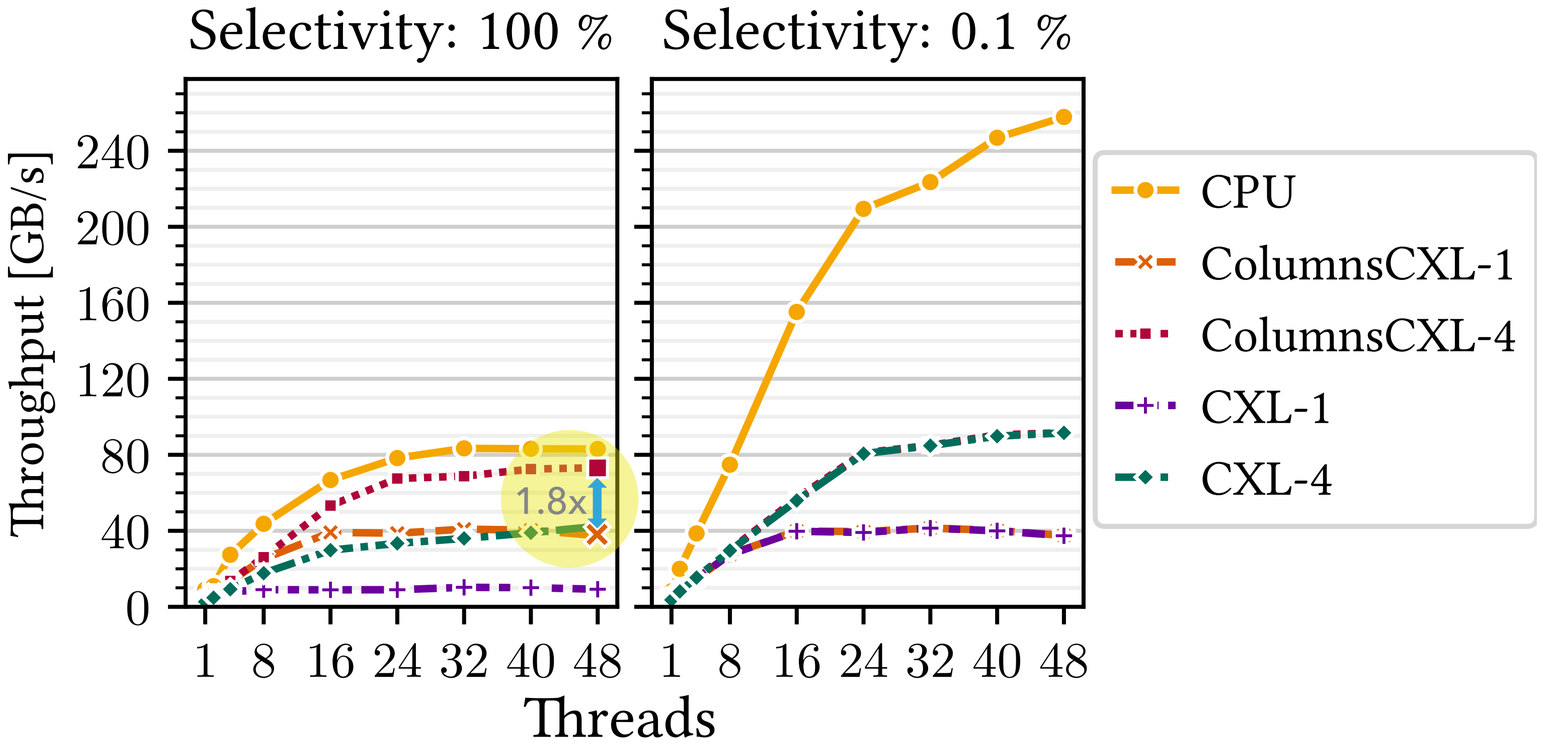

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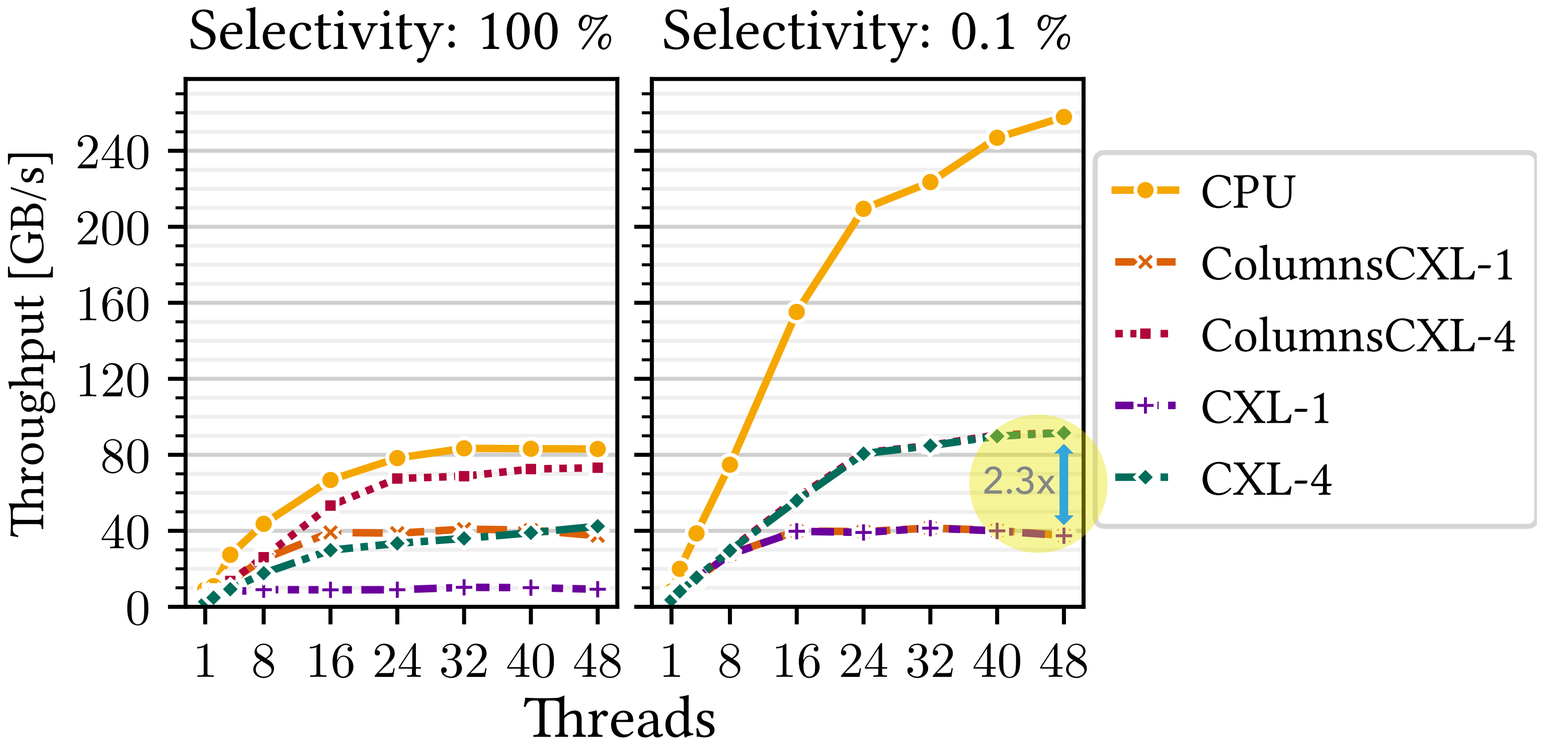

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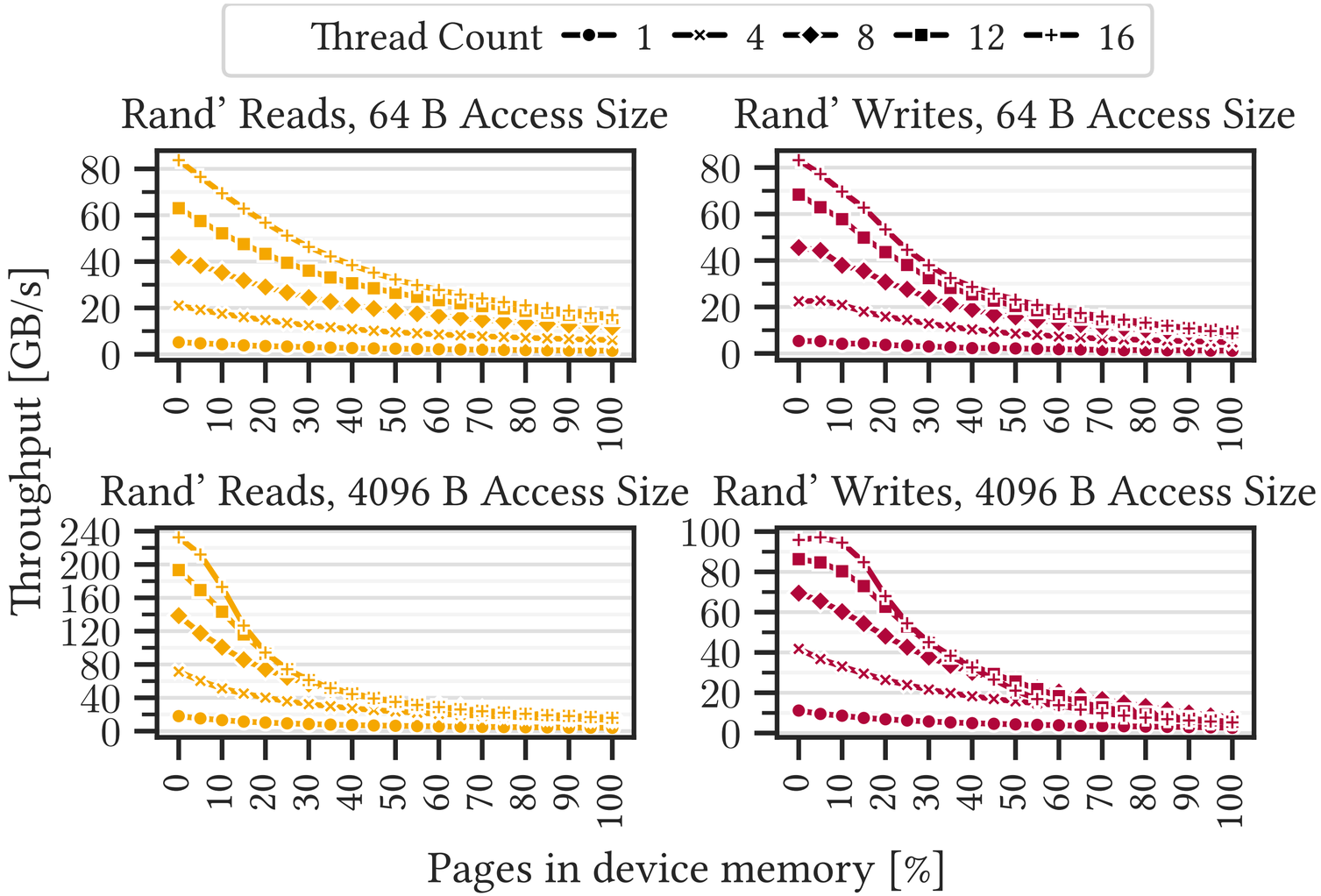
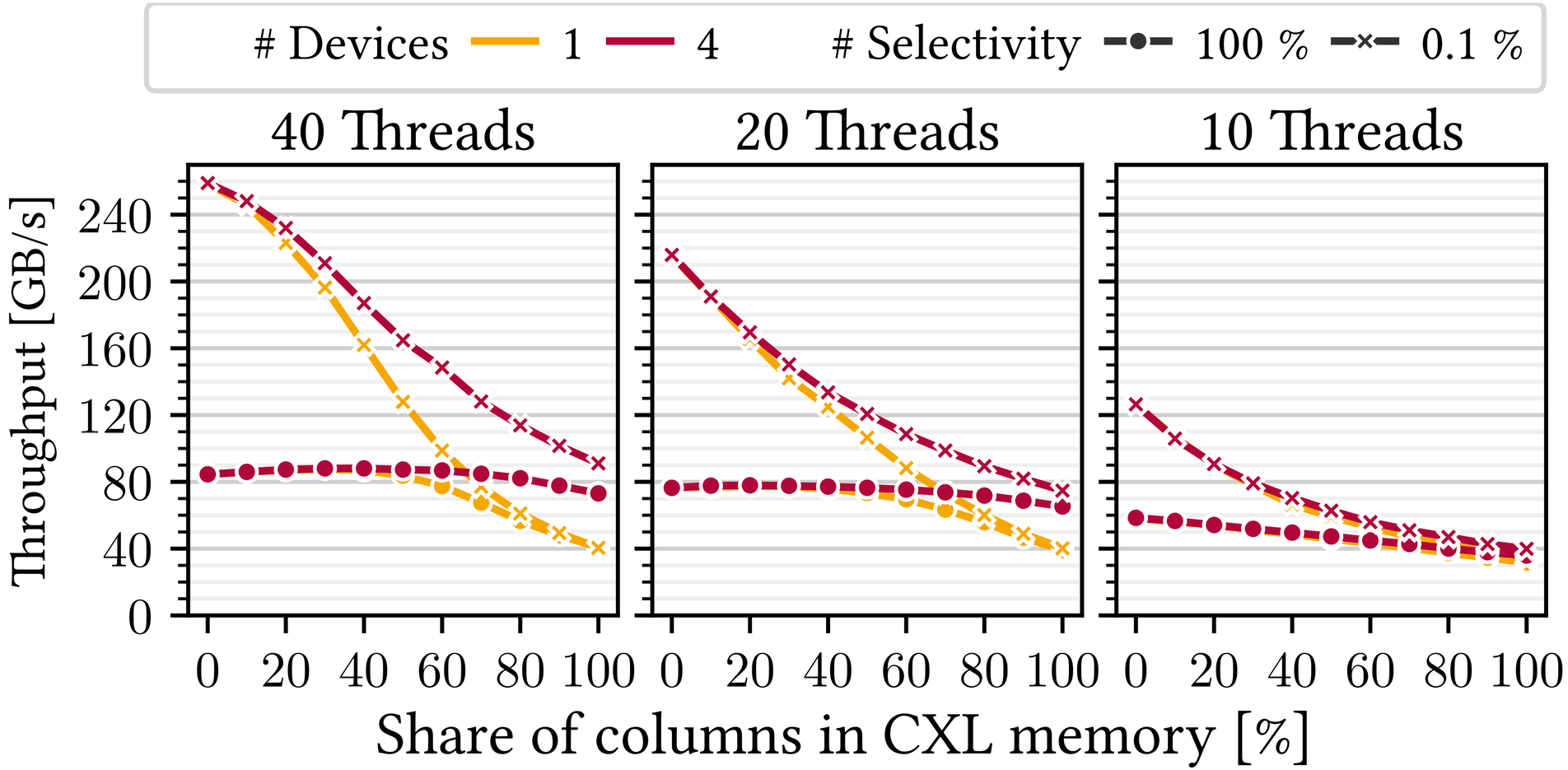
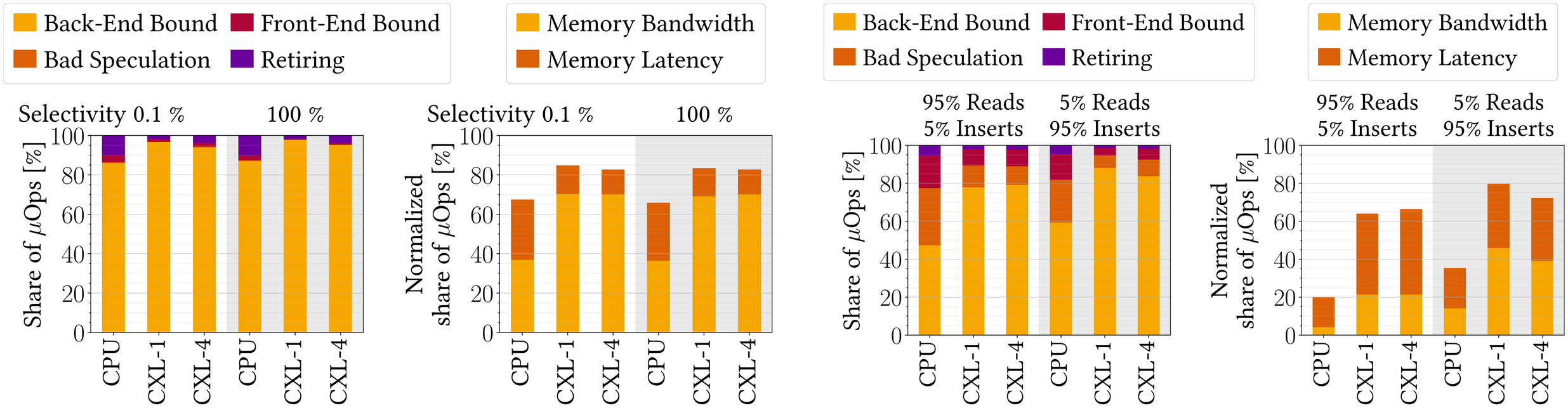
Impact of Storing Pages in CXL Device Memory



Scans with a Share of Columns in CXL Memory

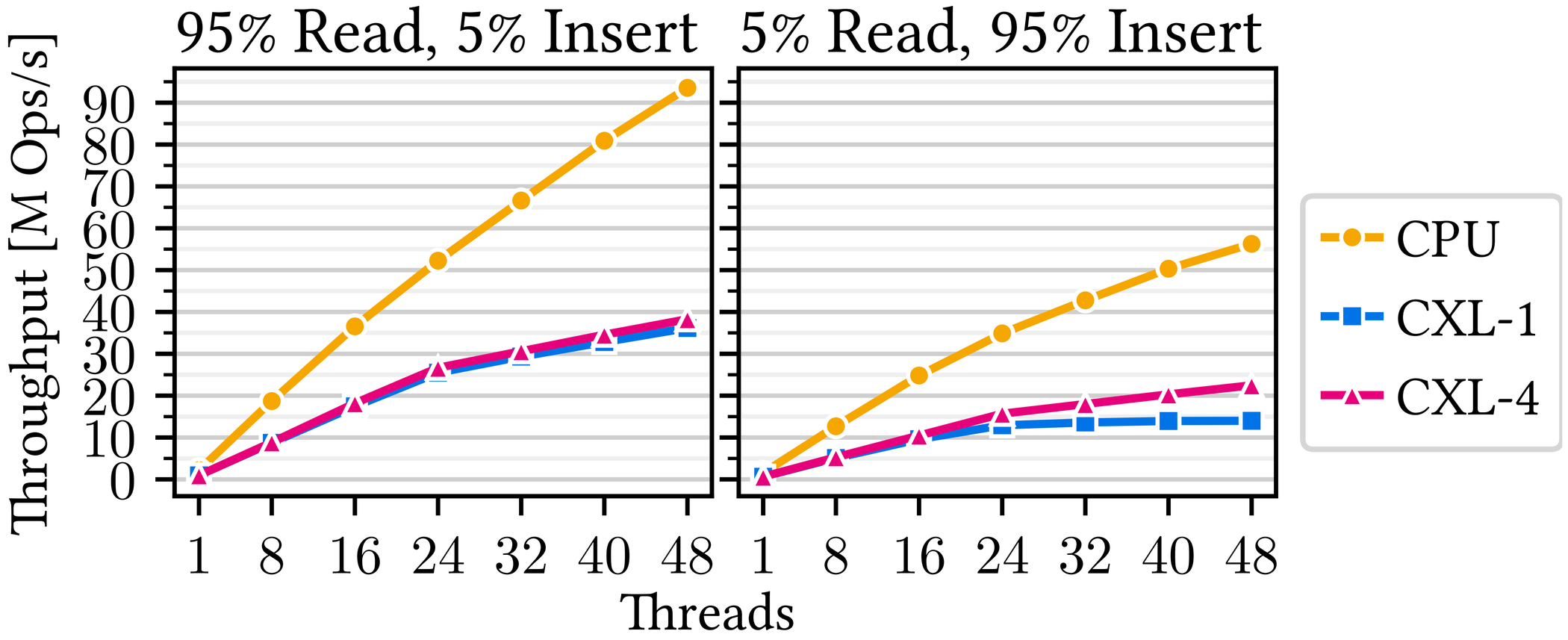


Top-Down Microarchitecture Analysis: Scans & B+-Tree Workloads

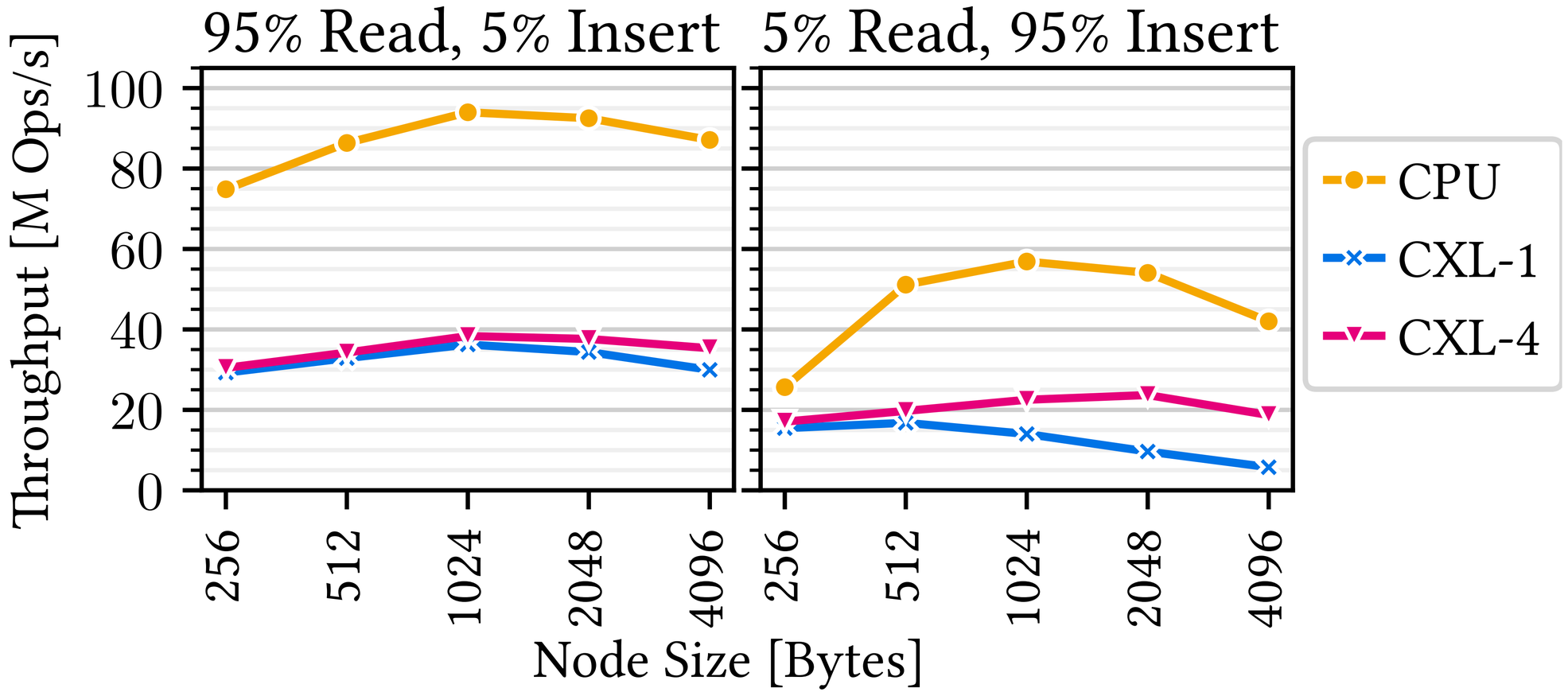


Performance breakdown with 40 threads and all data on one device (CXL-1), four devices (CXL-4), or CPU memory (CPU) with normalized bandwidth- and latency-bound shares.

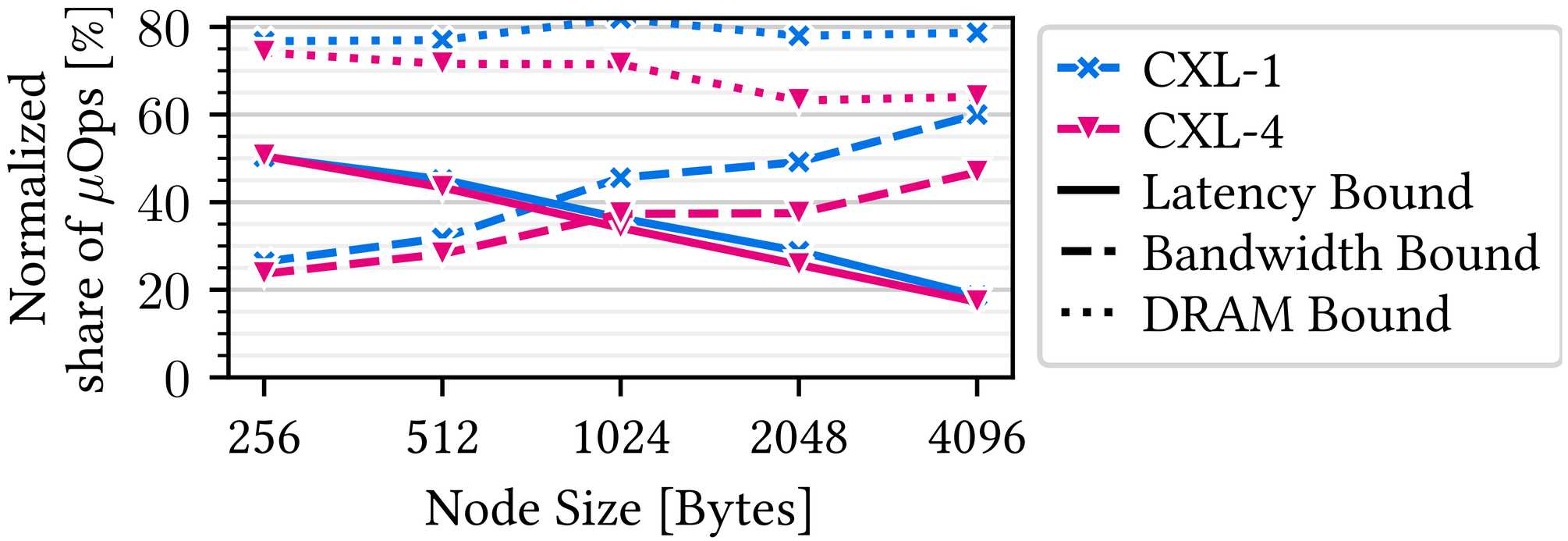
BTreeOLC Performance with Different Data Placement Configurations (1024 B Nodes)



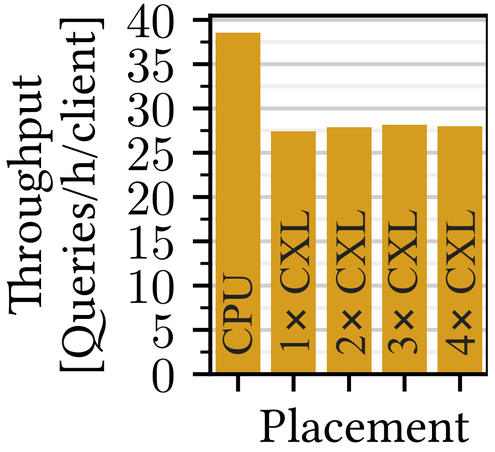
BTreeOLC Performance with Different Data Placements and Node Sizes for 48 Threads



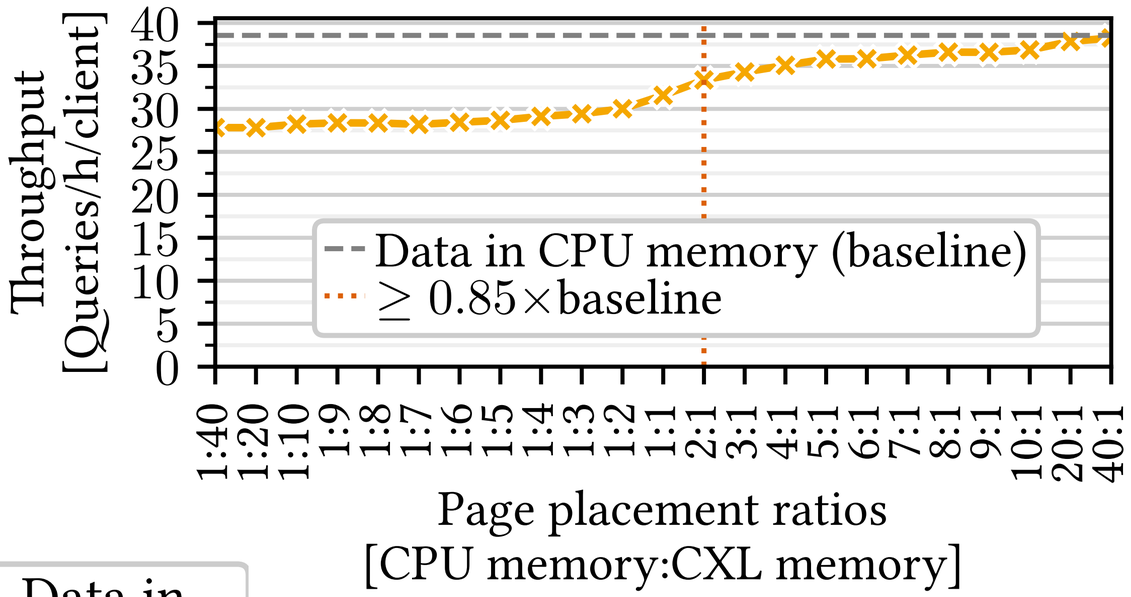
Latency- and Bandwidth-Bound μOps of the Write-Heavy Workload for Different Node Sizes



TPC-H on Hyrise



Black Box Approach (Page Granularity)



Access Frequency-Based (Column Granularity)